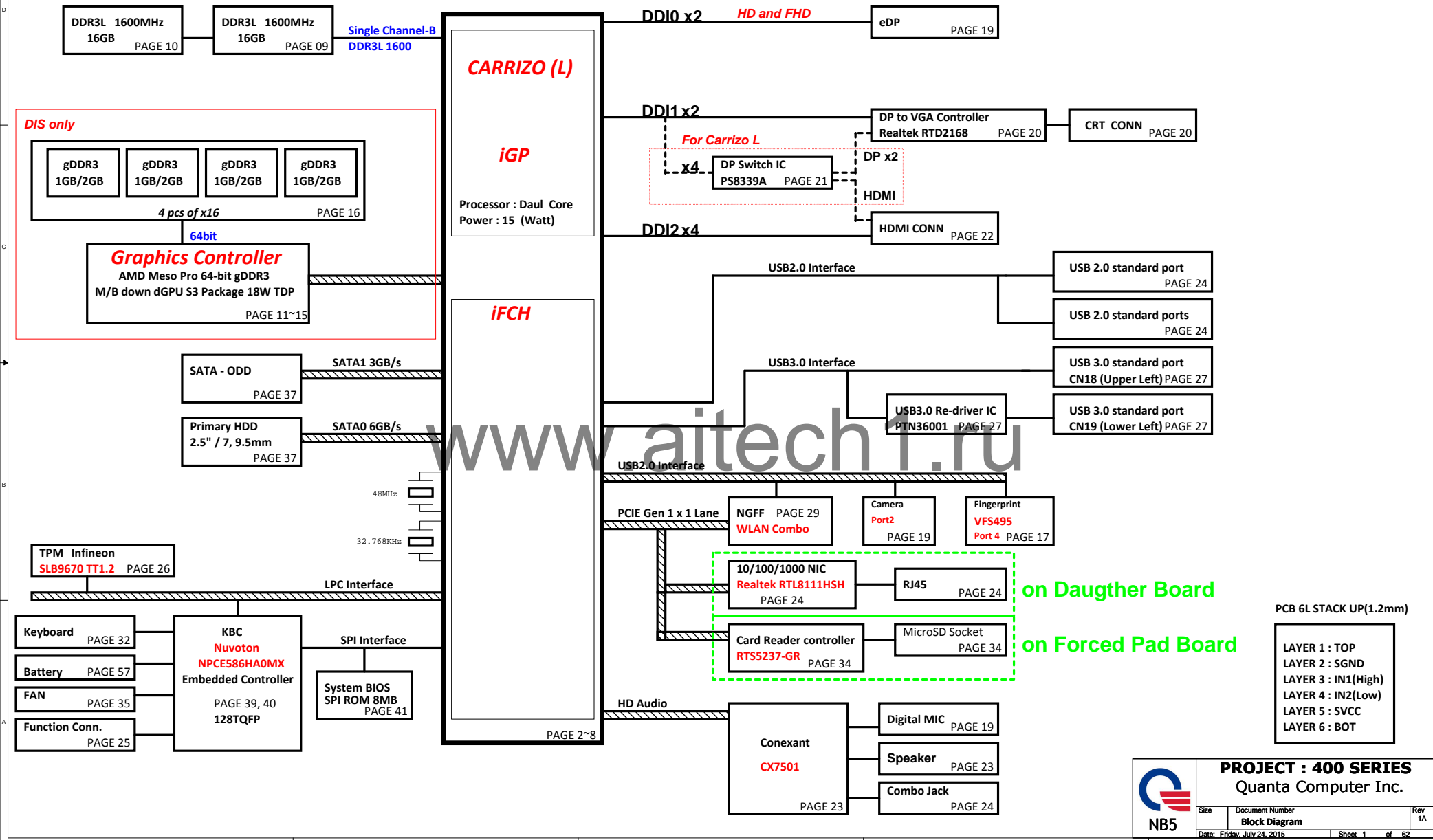


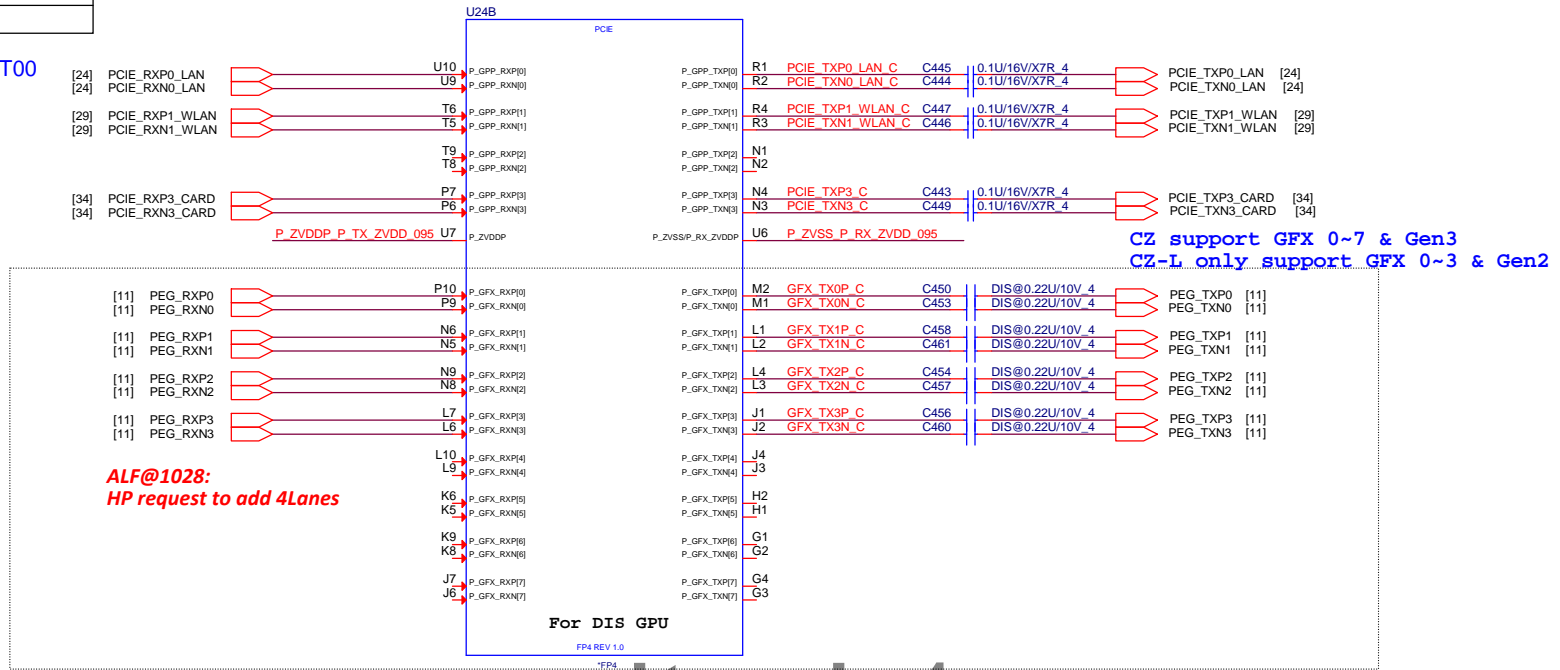
400 series Palazzo / X73A (UMA/DIS) Schematics

01



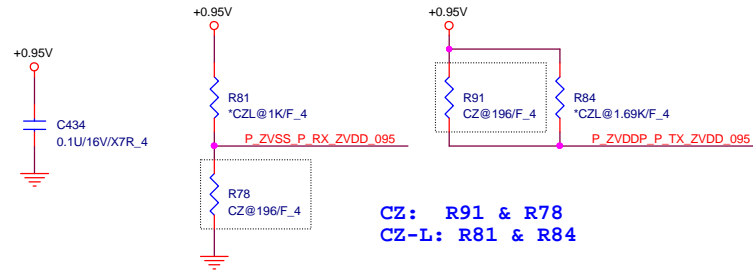
	QBCON	TOPBSQ
Carrizo	AJ1802CUT01	AJ1802CUT02

Carrizo DB phase use AJ1802CUT00



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Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4103K1B08

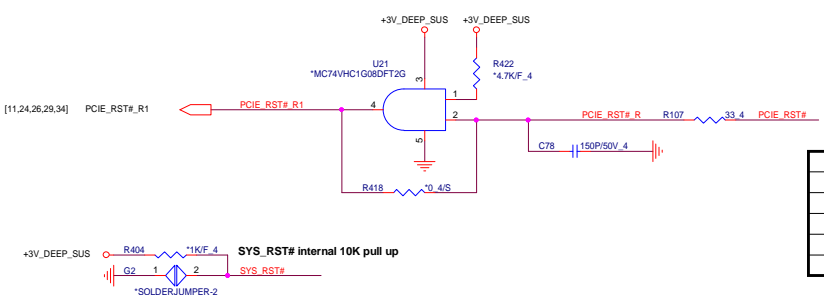


PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	Carrizo 1/7 (PCIE)	1A
Date: Friday, July 24, 2015	Sheet	of 62

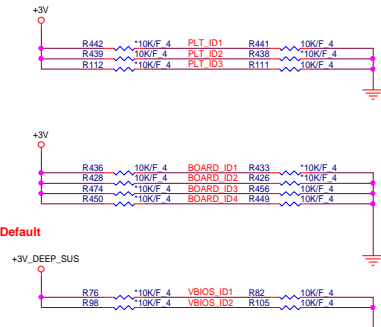
	PLT_ID1	PLT_ID2	PLT_ID3
	EGPIO95	EGPIO96	EGPIO101
Palazzo 15°	0	1	0

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
BOARD REVISION	EGPIO97	EGPIO98	EGPIO99	EGPIO100	
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SI8	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MY1	1	1	0	0	Default
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	

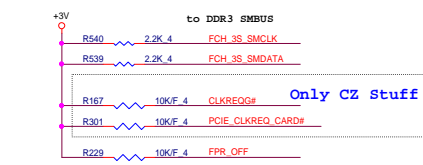
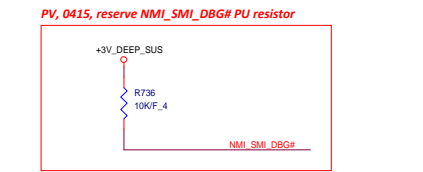


ALF@1110:
HP confirmed the 00 for DIS, 11 for UMA,
need to set in BOM

VBIOS_ID	VBIOS_ID1	VBIOS_ID2
	AGPIO6	AGPIO24
Discrete VRAM Group #1	0	0
Discrete VRAM Group #2	0	1
Discrete VRAM Group #3	1	0
UMA	1	1

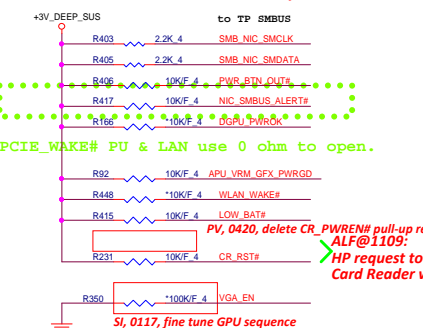


ALF@1110:
HP confirmed Okay!!

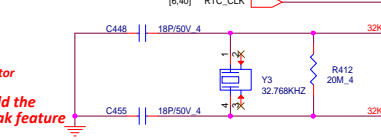


ALF@1119:
Reserved the CLKREQG# for dGPU

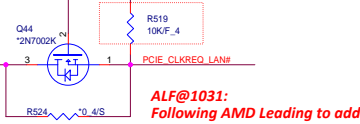
**PV, 0420, change NMI_SMI_DBG#
from AGPIO86 to AGPIO17, and delete CR_PWREN#**



for GPIO145~148
CZ pop those resistor
CZ-L can NC them

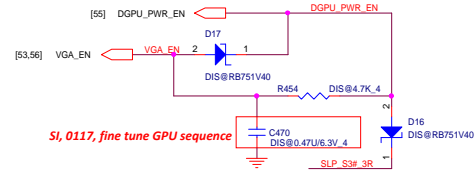


1029@RNY: Add PU for LAN CLKREQ#

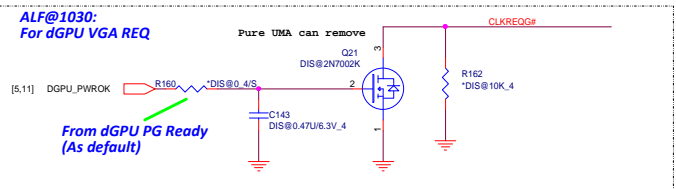


ALF@1031:
Following AMD Leading to add LS

ALF@1030:
For dGPU Power Enable Sequence & GPIOs



SI, 0117, fine tune GPU sequence



RNY@1108: Changed LANLINK# to PU ✓

ALF@1107:  WOL_EN
Changed WOL_EN and PD

Only CZ Stuff if no used

TP13
TP5

SI, 0201, reserved for fine tune GPU sequence

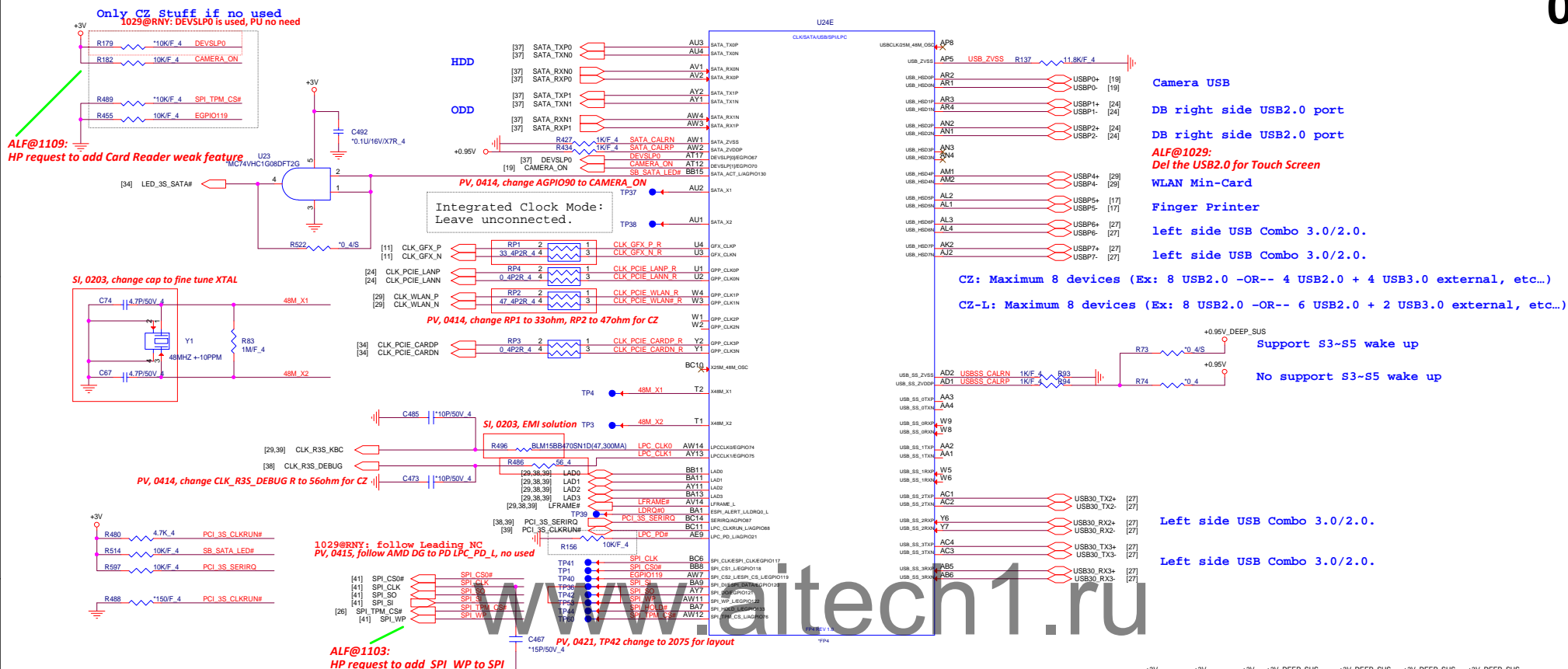
PV, 0414, change ACCEL_INTH GPIO pin and Pull-up power rail

*10K/F_4

Only CZ-L Stuff if no used
SI, 0201, fine tune GPU sequence

Follow AMD checklist 53537_1_03 suggestion to stuff R118/R120/R122

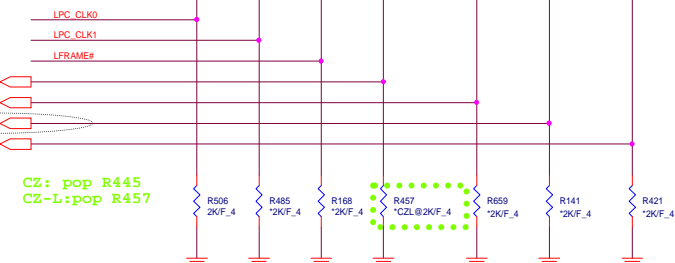
TEST2	TEST1	TEST0	Description
0	0	0	FCH JTAP accessible from APU when TAPEN is asserted FCH JTAP pins are overloaded for multiple functions, in this configuration the FCH JTAP are used as non-JTAP pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAP multi-function pins are configured as JTAP pins, in this configuration the FCH JTAP can be accessed from FCH JTAP pins
1	TMS	1	Use on ATE only Yuba JTAP enabled



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

1024@Ronny: AGPIO11 STRAP?



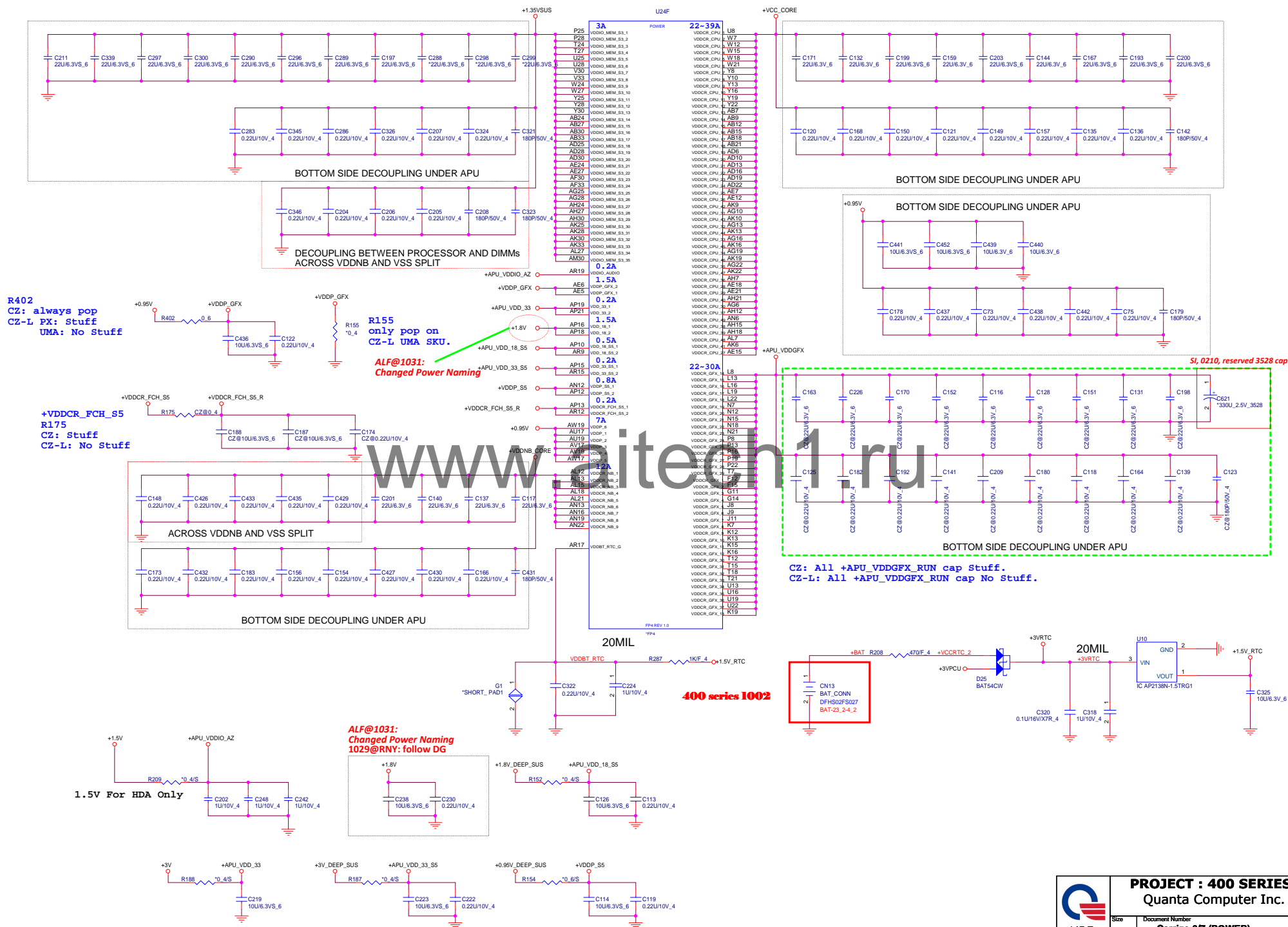
REQUIRED STRAPS

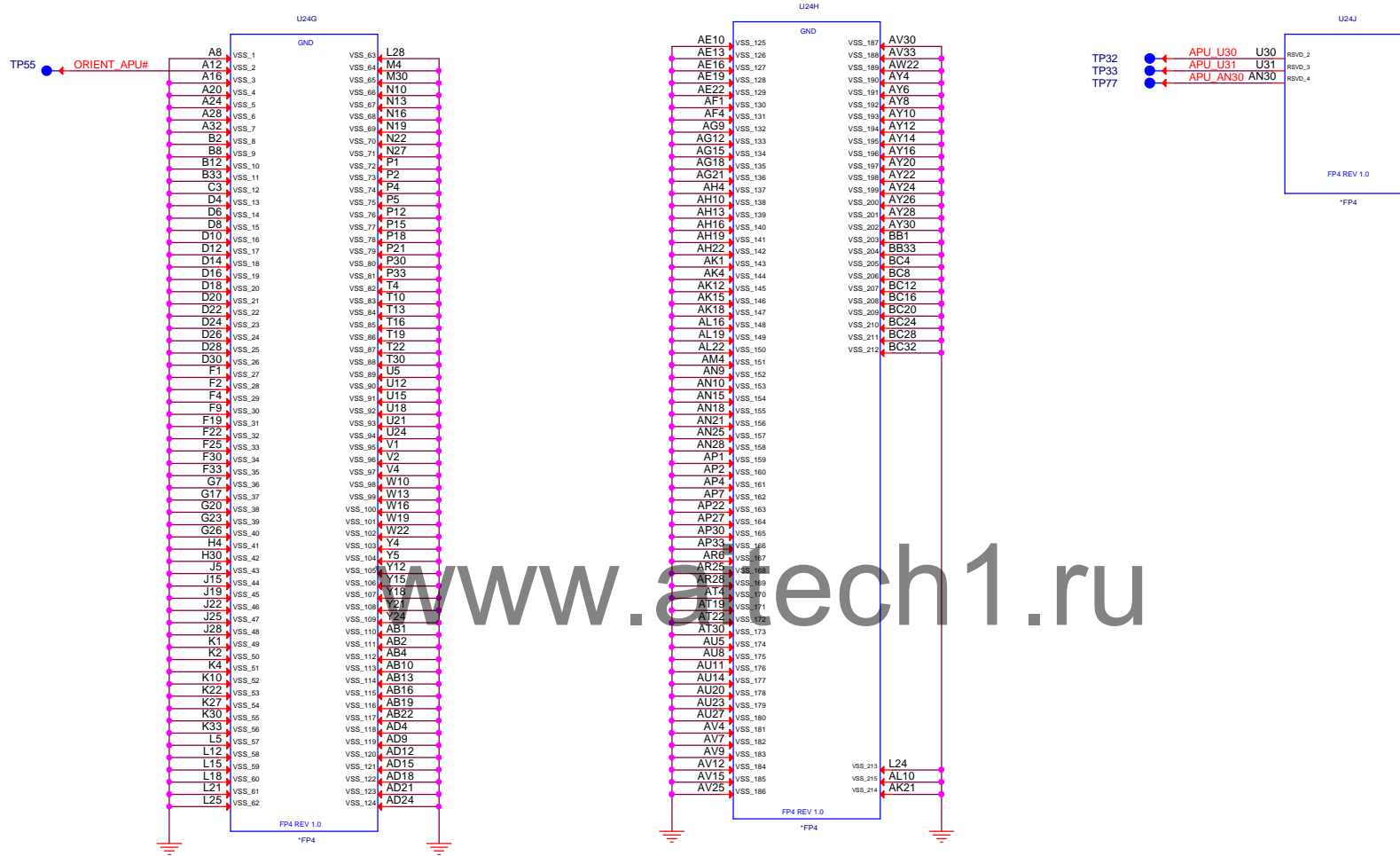
	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 In Pull-Up	RTC_CLK In Pull-Up	AGPIO11 BLINK In Pull-Up	SYS_RST# In Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM Enhanced reset logic (for quicker S5 resume) DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#LDT_PWRGD output to APU DEFAULT	normal reset mode output to APU DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100MHz PCIe clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM Default to traditional reset logic DEFAULT	Coin battery is not on board.	LDT_RST#LDT_PWRGD output to Pads	short reset mode output to Pads



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Quanta Computer Inc.

Size Document Number
Carrizo 5/7 (SATA/USB/SPI)
Date: Friday, July 24, 2015 Sheet 6 of 62





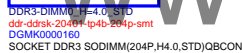
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	Carrzio 7/7 (GND)	1A
Date: Friday, July 24, 2015	Sheet 8 of 62	

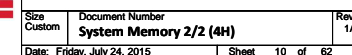


B



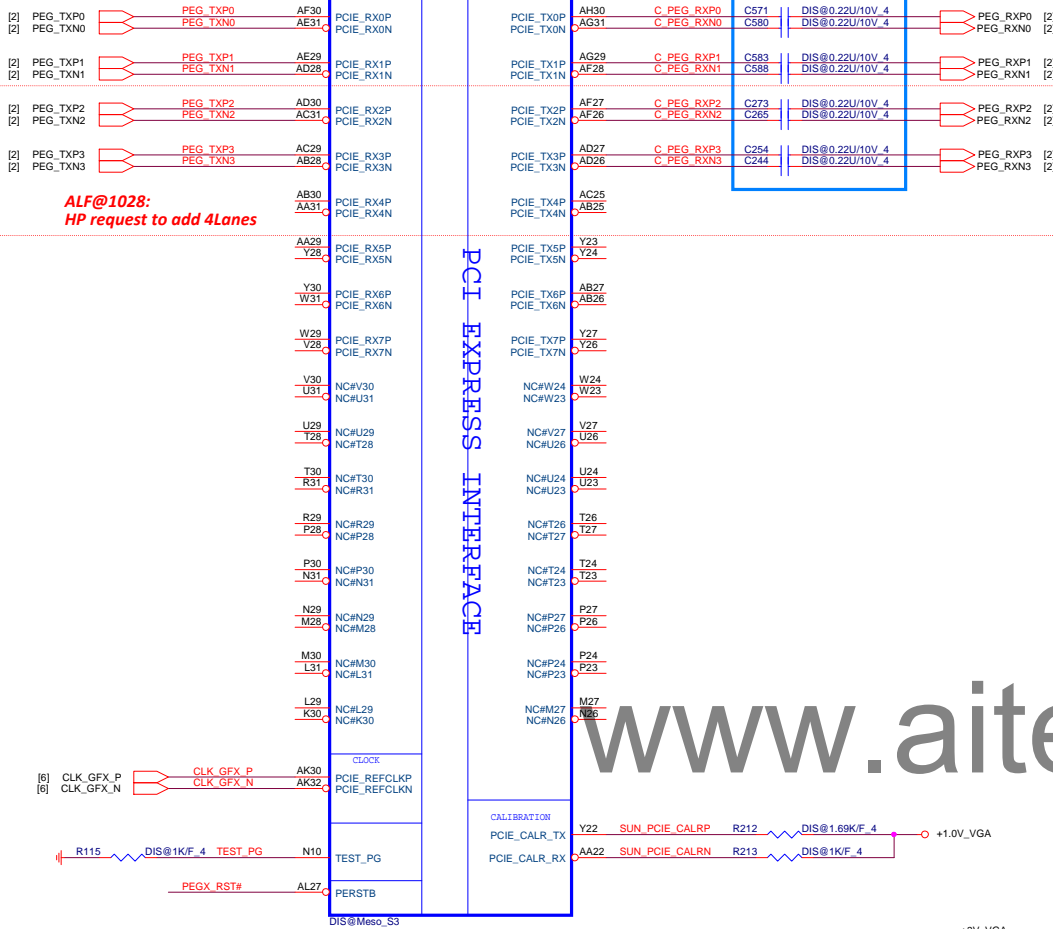


53537_105 change:
Type 1: and Type 2: from 1K/2 voltage

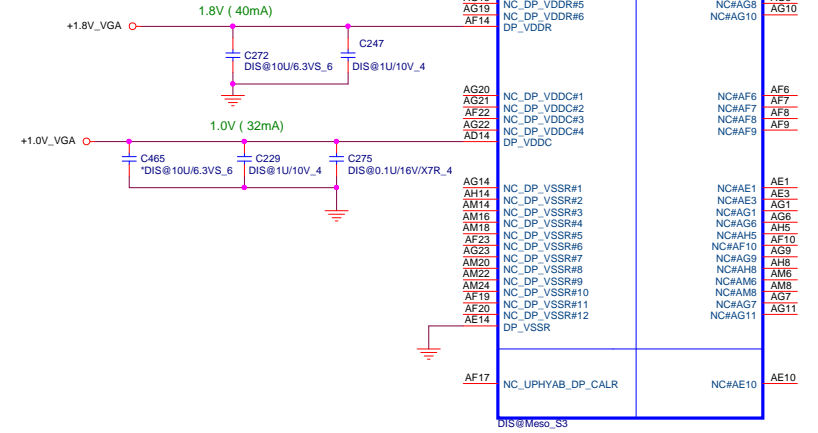


Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4103K1B08

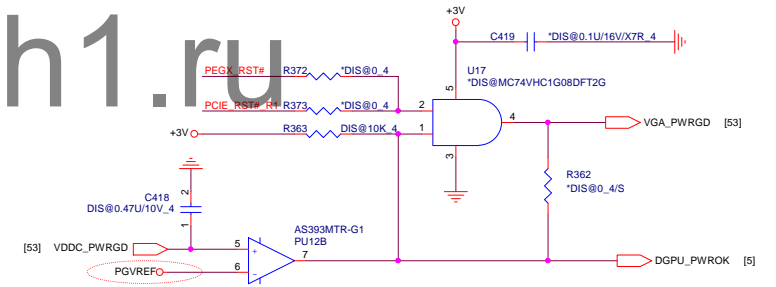
9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)



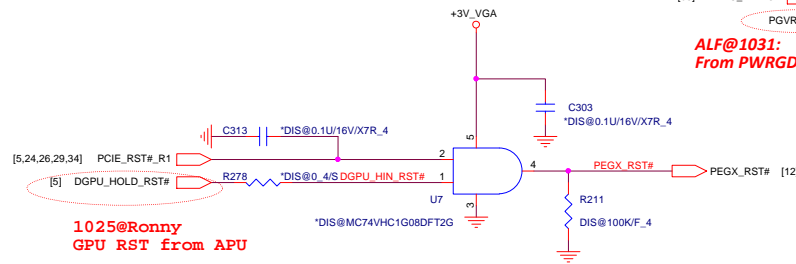
ALF@1028:
HP request to add 4Lanes



ALF@1031:
Following the 2014 AMD Leading Schematic for DGPU_PWROK

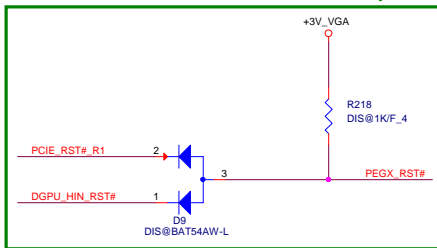


ALF@1031:
From PWRGD Generator



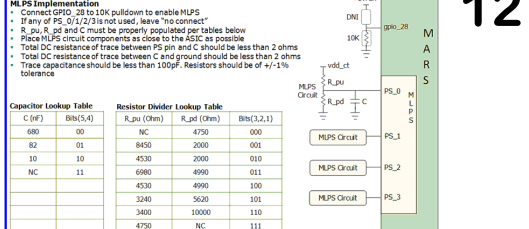
1025@Ronny
GPU RST from APU

12/10:reserve for verify



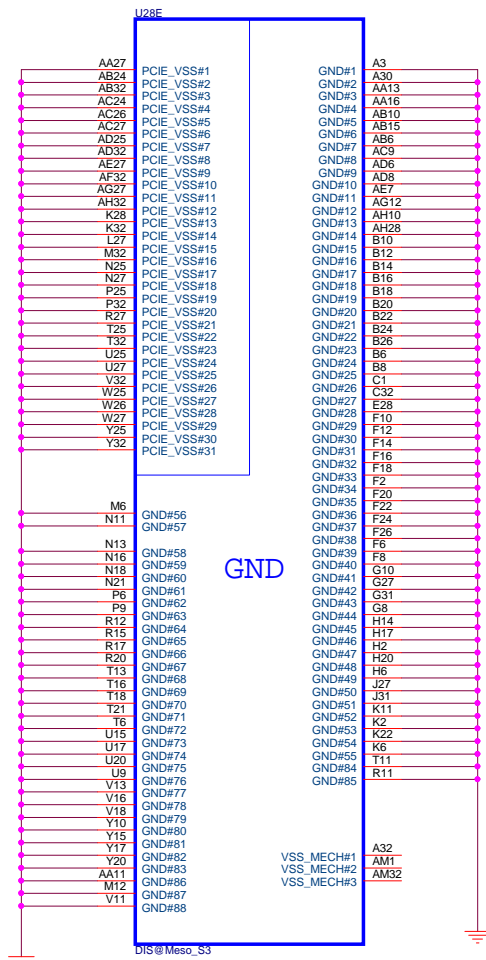
[12,14,53,55] +3V_VGA
[12,14,53,55] +1.8V_VGA
[14,55] +1.0V_VGA

NB5	PROJECT : 400 SERIES		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	TOPAZ S3 PCIE/DP power	1/1	
Monday, July 28, 2015		Sheet	11 of 62



Size of the Primary Memory Apertures	ROM_CONFIG2[9]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

PS_3[3:1]		Vendor	Type	Vendor P/N	QCT P/N (BS/QCCON)	PU	PD
000		Samsung- Q die	128Kx16 *4,1000Mhz	K4W6G146G-BCLA	AKDSMGST508/AKDSMGST509	NC	4.75K
001		Samsung- E die	256Kx16 *4,1000Mhz	K4W6G146E-BCLA	AKDSPGDT500/AKDSPGDT501	8.45K	2K
010		Hynix- Huma F die	128Kx16 *4,1000Mhz	HS7C936JFFR-11C	AKDSMD2W02/AKDSMD2W03	4.53K	2K
011		Hynix- C(Polaris)	256Kx16 *4,1000Mhz	HS7C496J3FR-NOG	AKDSPD2W01/AKDSPD2W02	6.96K	4.99K
100		Micron- K die	128Kx16 *4,1000Mhz	MT47L128M16J7-093G0	AKDSMGSTL6/AKDSMGSTL7	4.55K	4.99K
101		Micron- E die	256Kx16 *4,1000Mhz	MT47L256M16HA-093G0	AKDSPESTL00/AKDSPESTL01	3.24K	5.62K
110		Nanya- F die	128Kx16 *4,1000Mhz	N75CB128M16FP-PL	AKDSMGDTF00/AKDSMGDTF01	3.4K	10K
111		Nanya- D die	256Kx16 *4,1000Mhz	N75CB256M16DP-PL	AKDSPGDTF02/AKDSPGDTF03	4.75K	NC
Vendor id	VRAM density	Meso Multi-level Pin Straps					
00 = Samsung	0=128Mx16	WLP8 Bit; PS_3					
01 = Hynix	1=256Mx16	Mappings between the bit values and resistor values					
10 = Micron							
11 = Nanya							



U28F

LVDS_CONTROL

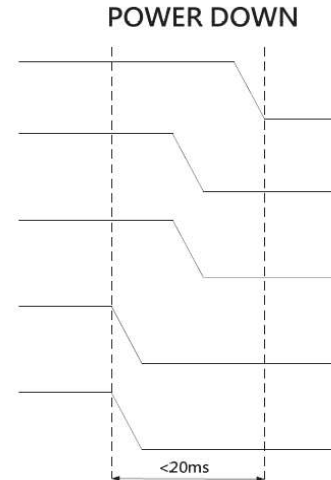
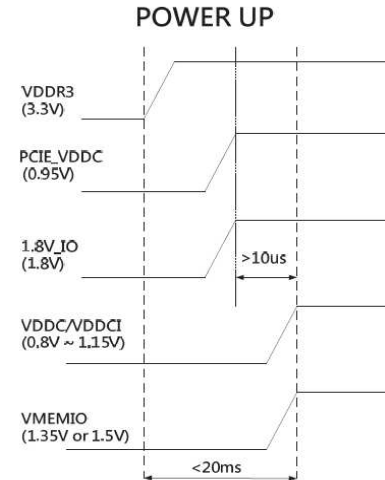
NC_UPHYAB_TMDPA_TX0N
NC_UPHYAB_TMDPA_TX0P
NC_UPHYAB_TMDPA_TX1N
NC_UPHYAB_TMDPA_TX1P
NC_UPHYAB_TMDPA_TX2N
NC_UPHYAB_TMDPA_TX2P
NC_UPHYAB_TMDPA_TX3N
NC_UPHYAB_TMDPA_TX3P
NC_TXOUT_L3P
NC_TXOUT_L3N
NC_TXOUT_U3P
NC_TXOUT_U3N

TMDP

NC_UPHYAB_TMDPB_TX0N
NC_UPHYAB_TMDPB_TX0P
NC_UPHYAB_TMDPB_TX1N
NC_UPHYAB_TMDPB_TX1P
NC_UPHYAB_TMDPB_TX2N
NC_UPHYAB_TMDPB_TX2P
NC_UPHYAB_TMDPB_TX3N
NC_UPHYAB_TMDPB_TX3P

DIS@ Meso_S3

POWER UP / POWER DOWN SEQUENCE



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	RESERVED	X
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYSN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

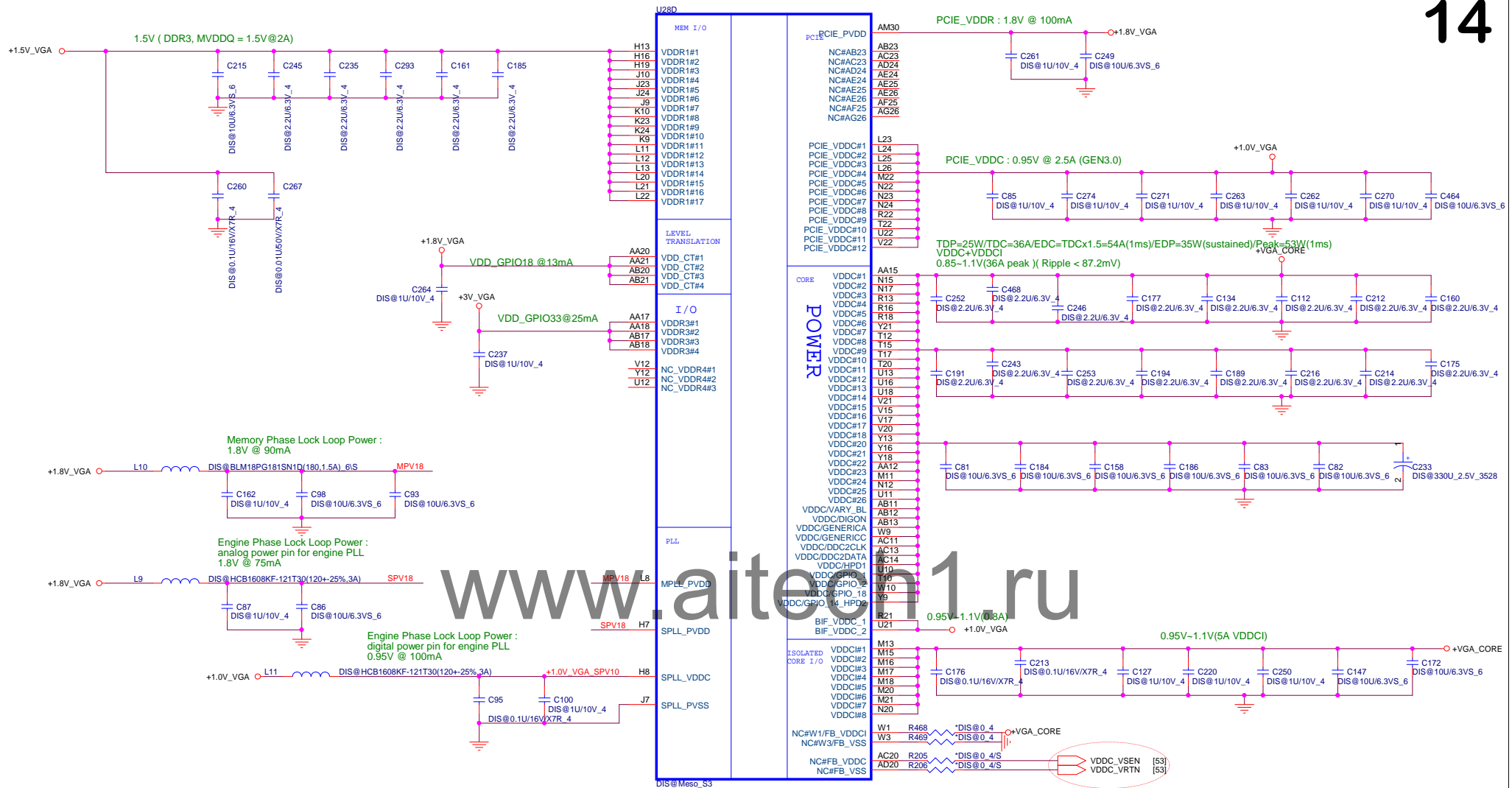
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2



PROJECT : 400 SERIES
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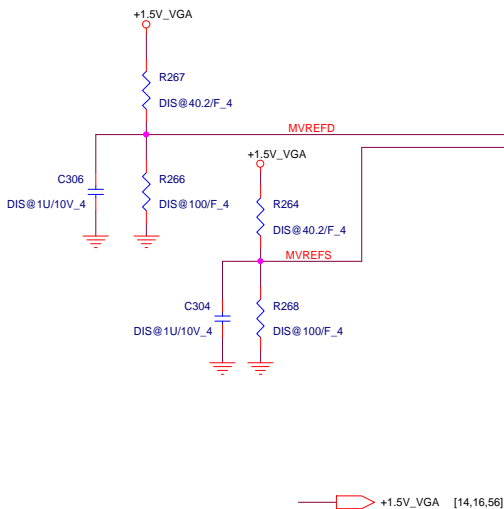
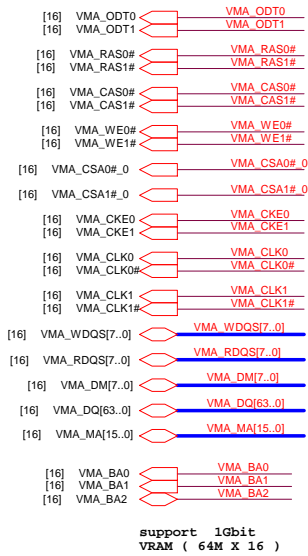
Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date:	Friday, July 24, 2015	Sheet 13 of 62



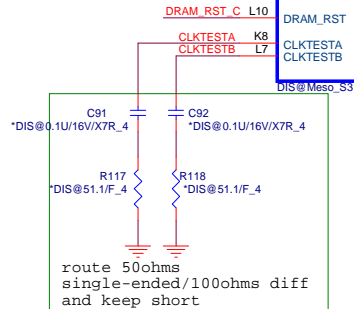
ALF@1029:
Follow Power Side



	PROJECT : 400 SERIES		
	Quanta Computer Inc.		
Size	Document Number	Rev	
	TOPAZ S3 Power	1A	
Date:	Friday, July 24, 2015	Sheet	14 of 62

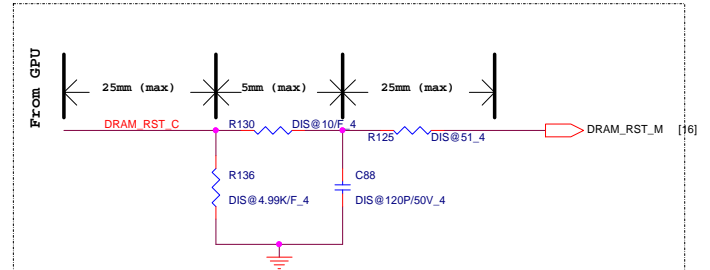
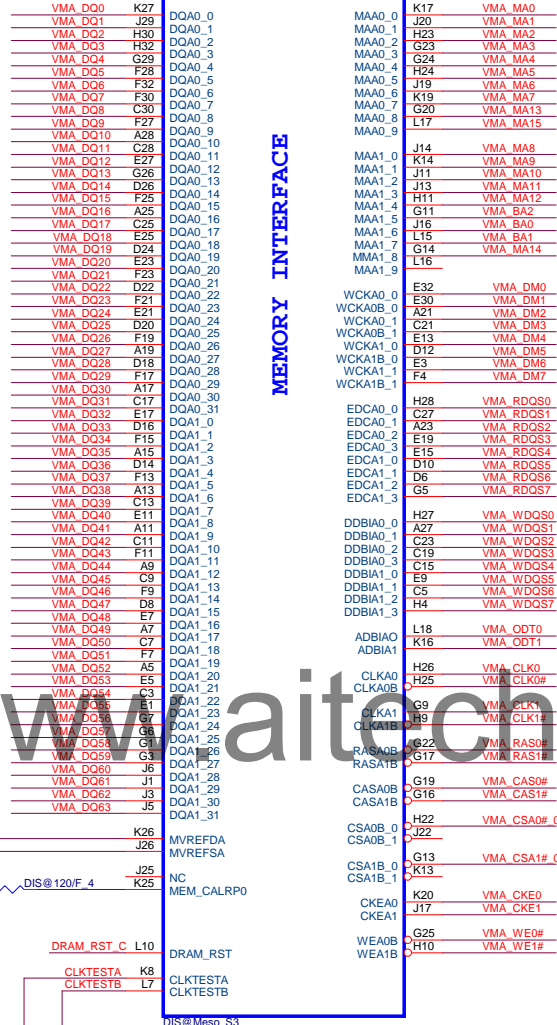


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U28C

MEMORY INTERFACE



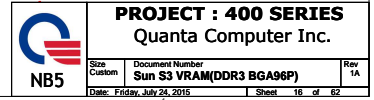
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

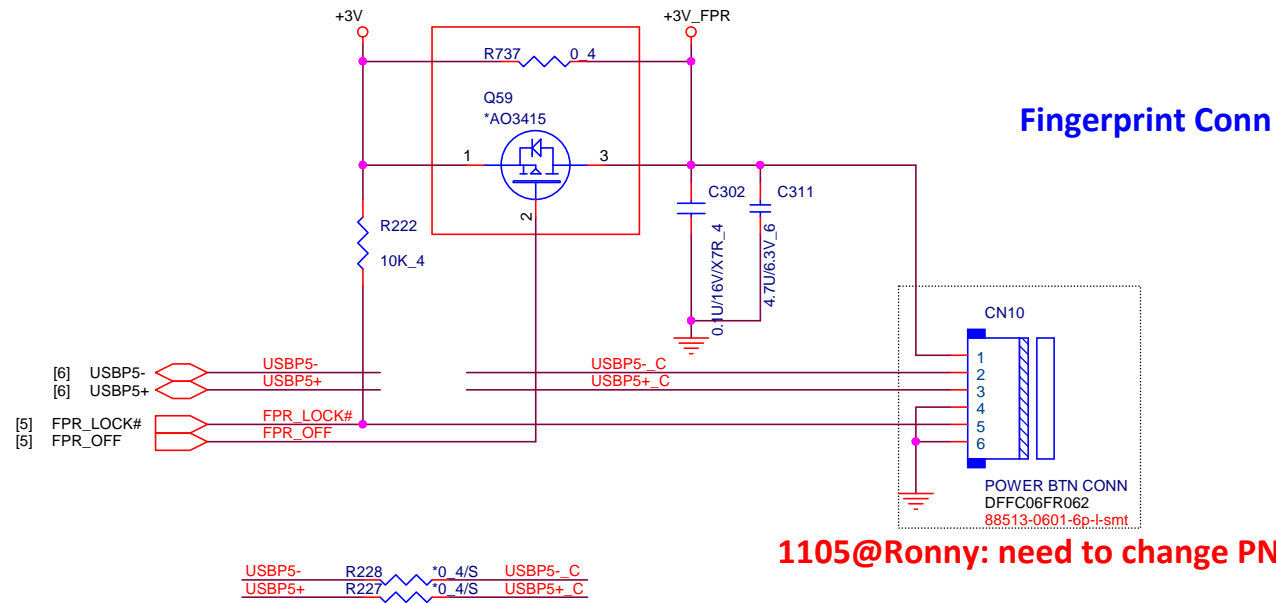


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Quanta Computer Inc.

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TPOAZ_S3_MEM_Interface
Date: Friday, July 24, 2015 Sheet 15 of 62



PV, 0415, follow leading project to add MOSFET for FPR_OFF



1105@Ronny: need to change PN and FP



400 series 0930 Delete DP DemultiPlexer due to not support docking

400 series 1001 change to LVDS/eDP co-design

18

ALF@1119:

HP confirmed to remove the eDP to LVDS convertor.

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[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58]

+3V



PROJECT : 400 SERIES
Quanta Computer Inc.

Size
Custom

Document Number
RTD2136

Rev
1A

Date: Friday, July 24, 2015

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LID Switch 400 series 1001 change LVDS/eDP co-design

19

LVDS Conn.

GS12401-1011-9H
lvs-50671-04041-001-40p-I

DFFC40R063

CN2

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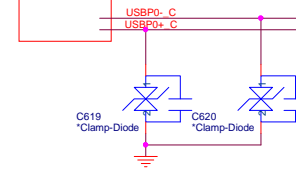
4

3

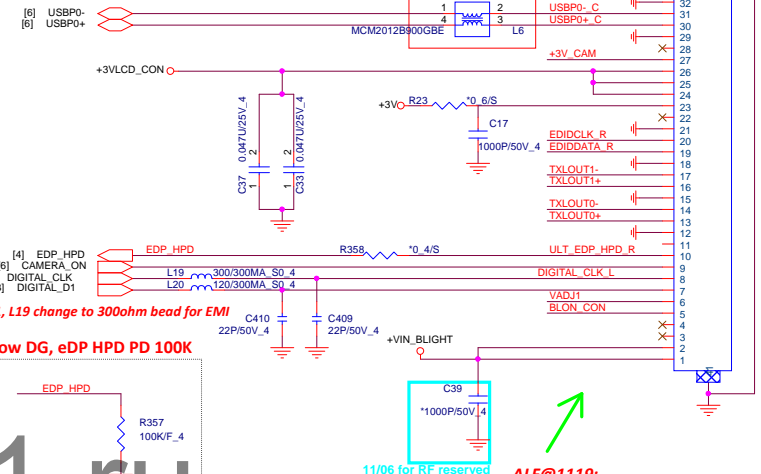
2

1

SI, 0209, EMI need to add CMC
PVR, 0720, delete USB2.0 0ohm co-lay



SI, 0209, EMI need to add CMC



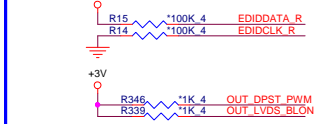
PV, 0421, L19 change to 300ohm bead for EMI

1029@RNY: follow DG, eDP HPDP PD 100K

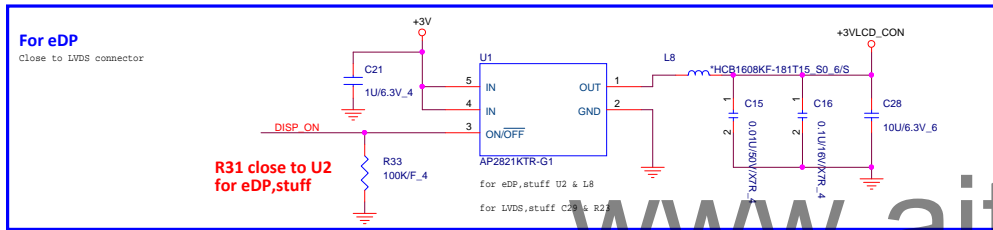
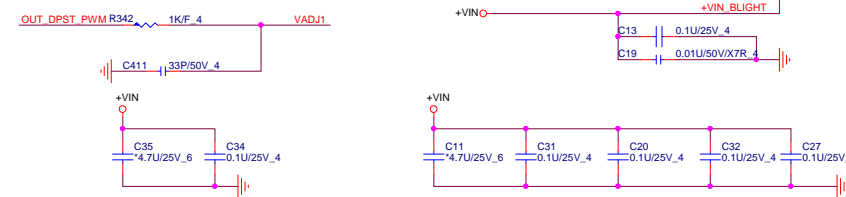
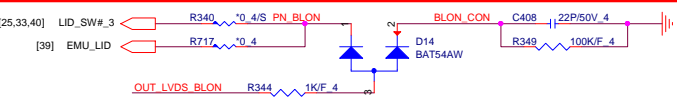
11/06 for RF reserved

ALF@1119:
1. Removed the LVDS Pin Define
2. Swapped Pin to sync up with 13"

For EDP Only: Reserved

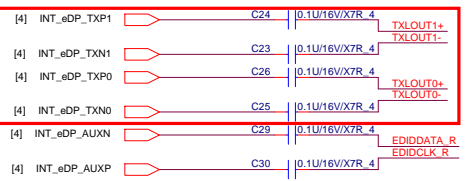


1124@RNY
Follow T/L BLON circuit
& avoid assembly ESD protection



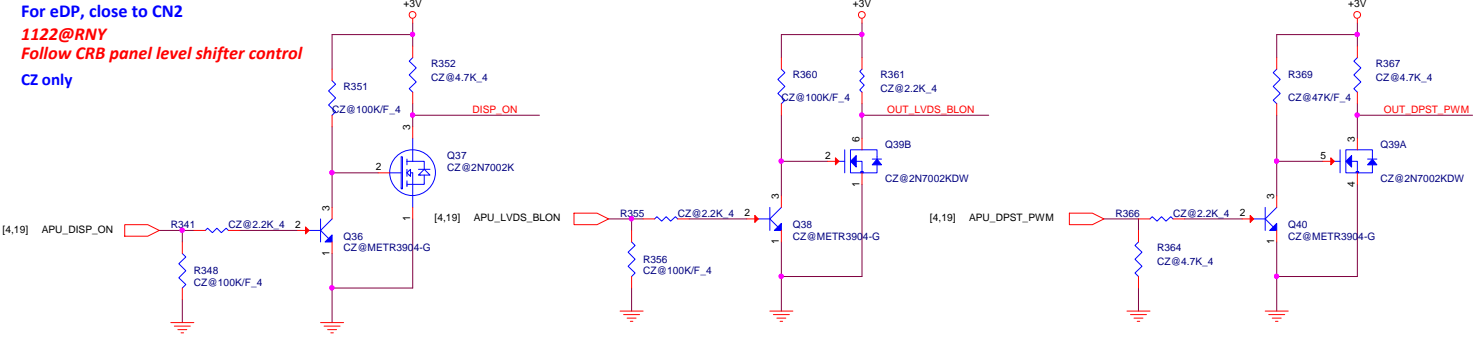
R31 close to U2
for eDP,stuff

For EDP Only: stuff Cap
For LVDS only stuff Resistor

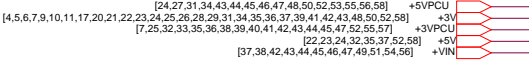
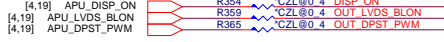


ALF@1113:
Swapped Pin to sync up with 13"

For eDP, close to CN2
1122@RNY
Follow CRB panel level shifter control
CZ only

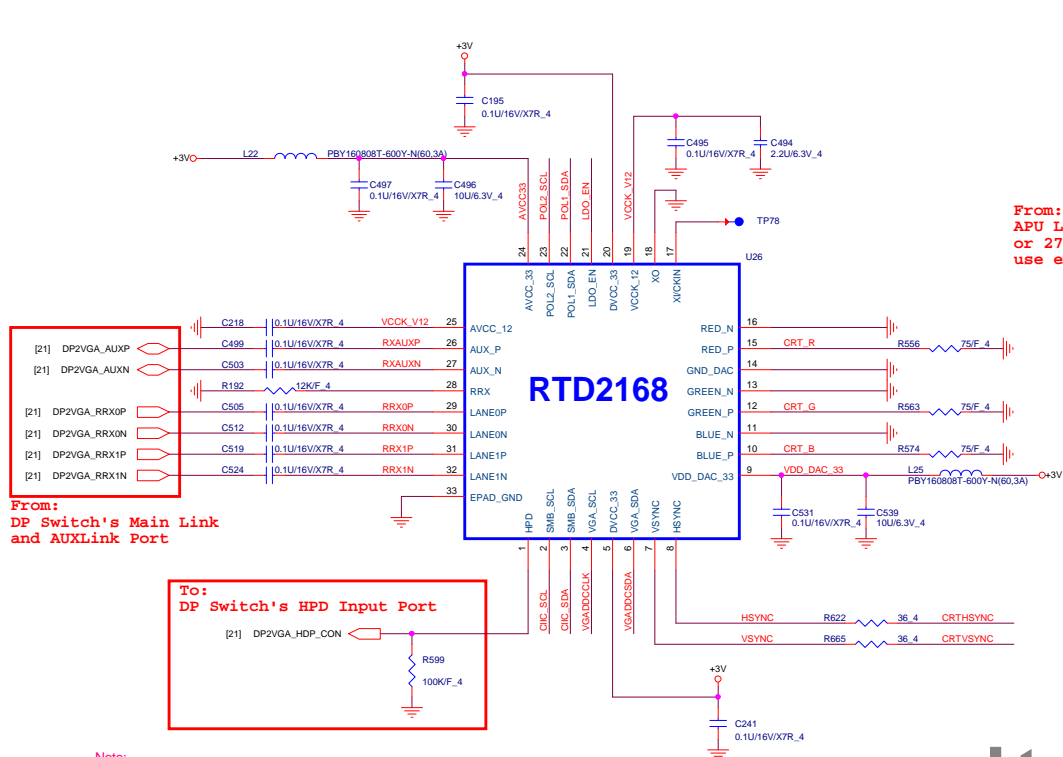


CZ-L only



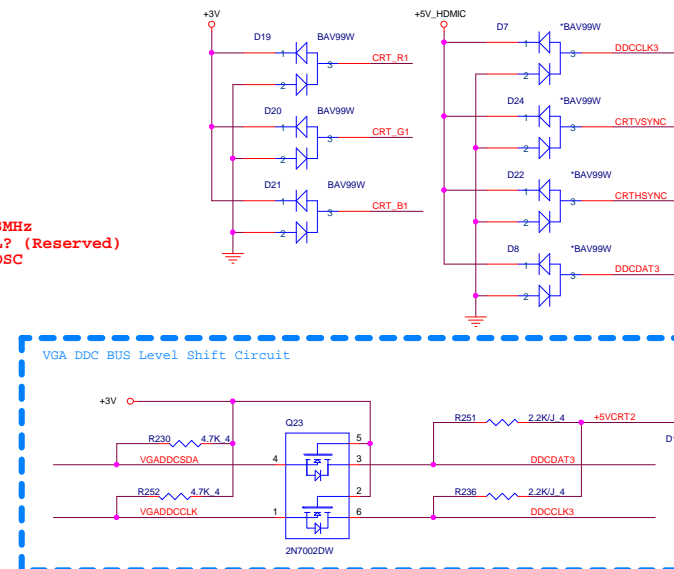
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/D-MIC	1A
Date: Monday, July 27, 2015	Sheet 19 of 62	

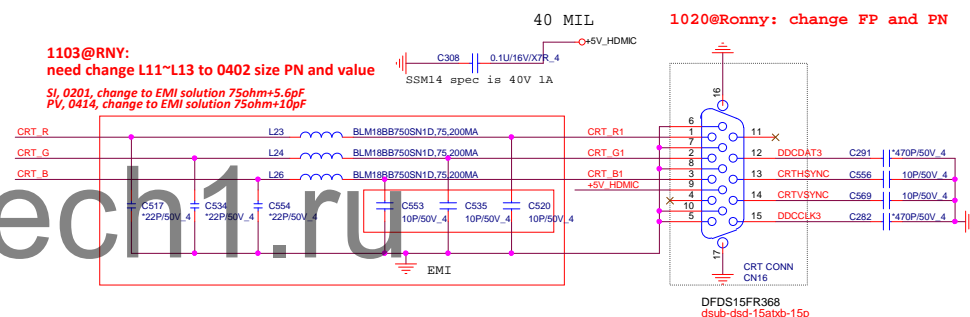


Note:

- 1- C1,C3,C6,C8,C9,C11,C12,C19,C20
Should be close to chip
- 2- C12 should be X5R material
- 3- R1 should be 12K ohm with +/-1%
- 4- R8, R9, R10 should be 75 ohm with +/-1%

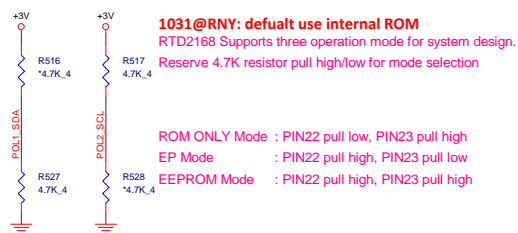


1103@RNY:
need change L11~L13 to 0402 size PN and value
SI, 0201, change to EMI solution 75ohm+5.6pF
PV, 0414, change to EMI solution 75ohm+10pF



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



EEPROM MODE

In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following conditions.

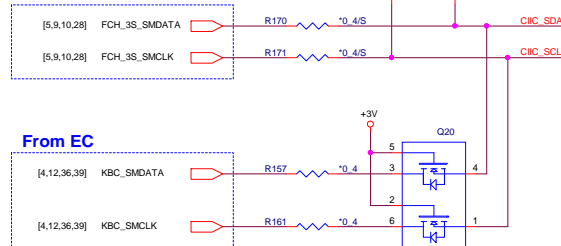
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

From PCH



Embedded LDO

Select VCKK V12 source from external 1.2V or embedded LDO

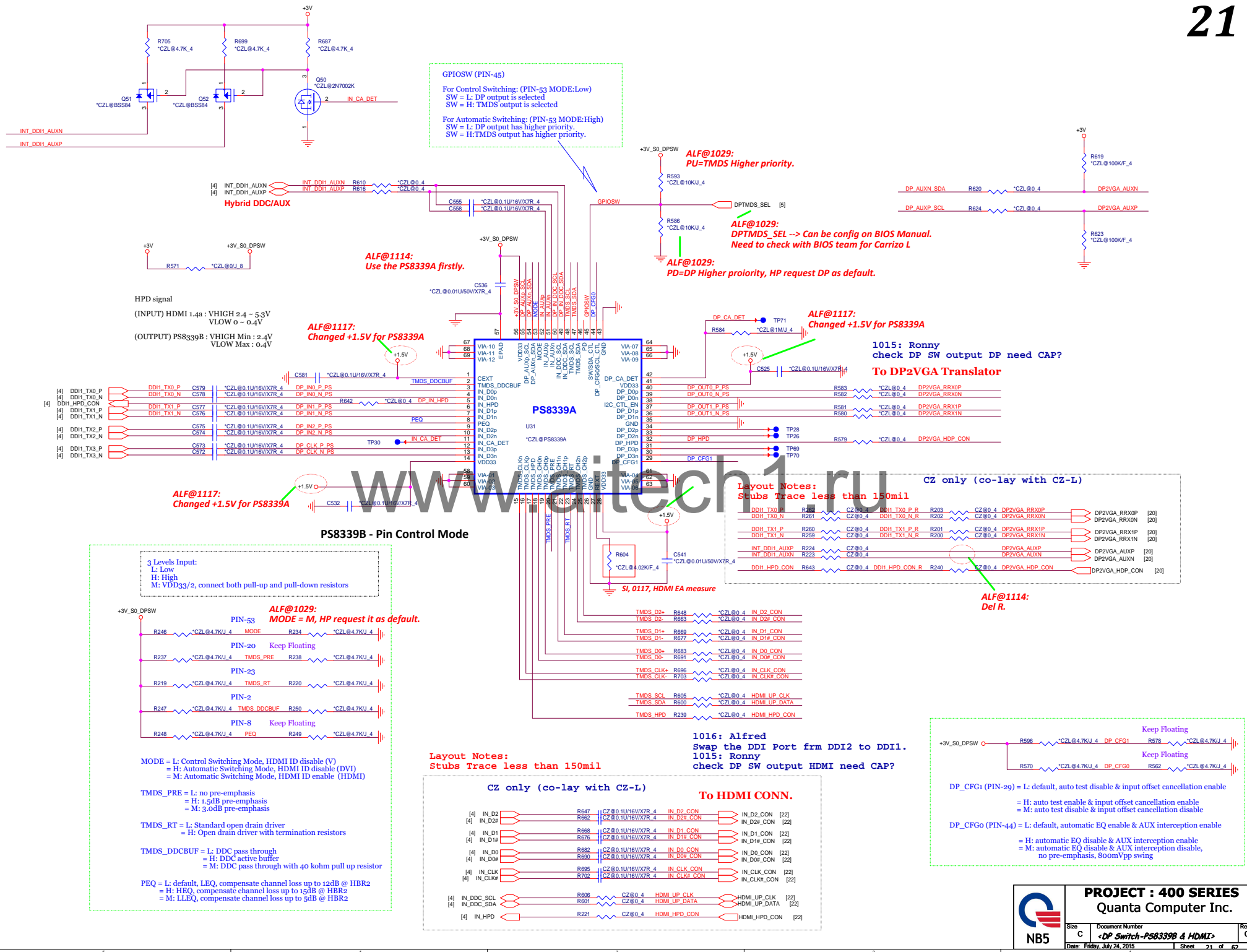


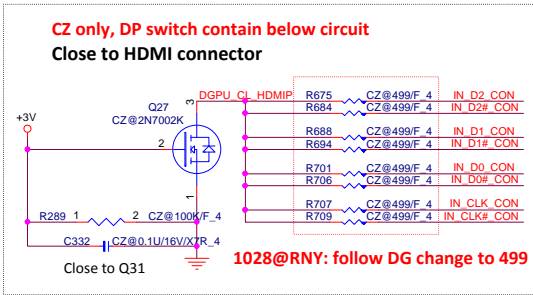
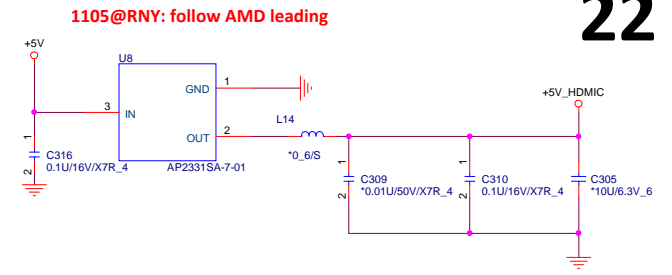
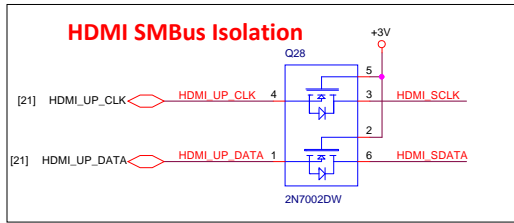
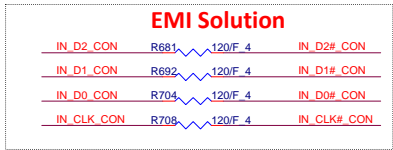
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO



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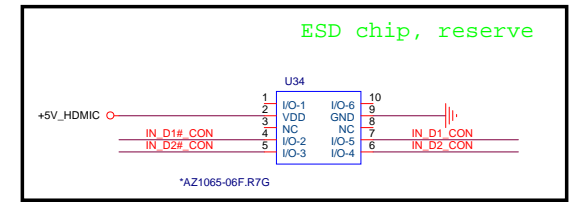
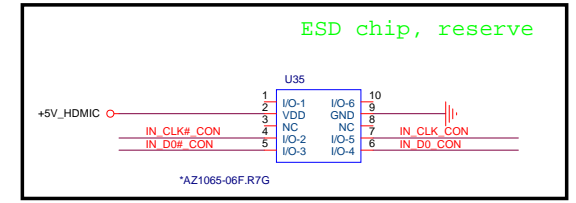
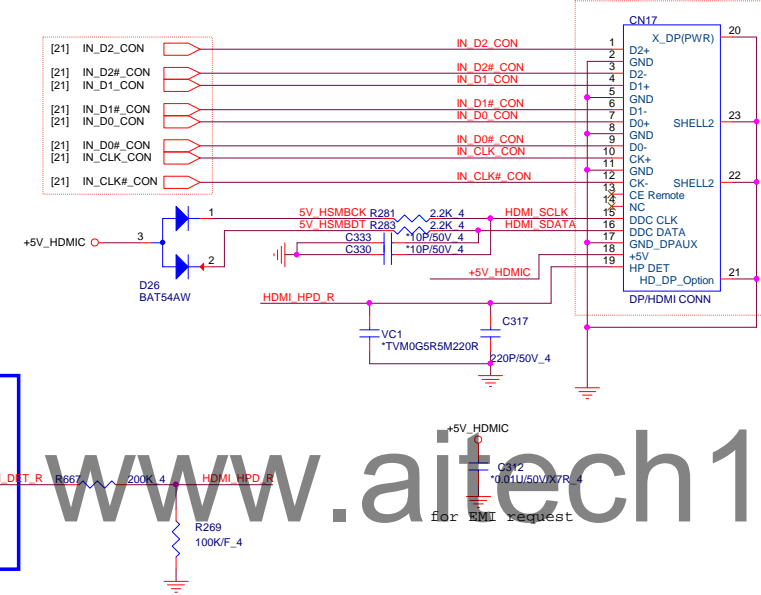
Size Custom	Document Number DP to VGA	Rev 1A
Date: Friday, July 24, 2015		Sheet 20 of 62



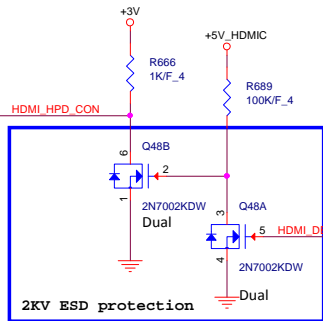


1014@Ronny : remove re-driver IC
1015@Ronny: Add DP Switch
1016@Alfred: Changed the DDI1 to DDI2

1028@Ronny : change FP only
need confirm PN then change PN

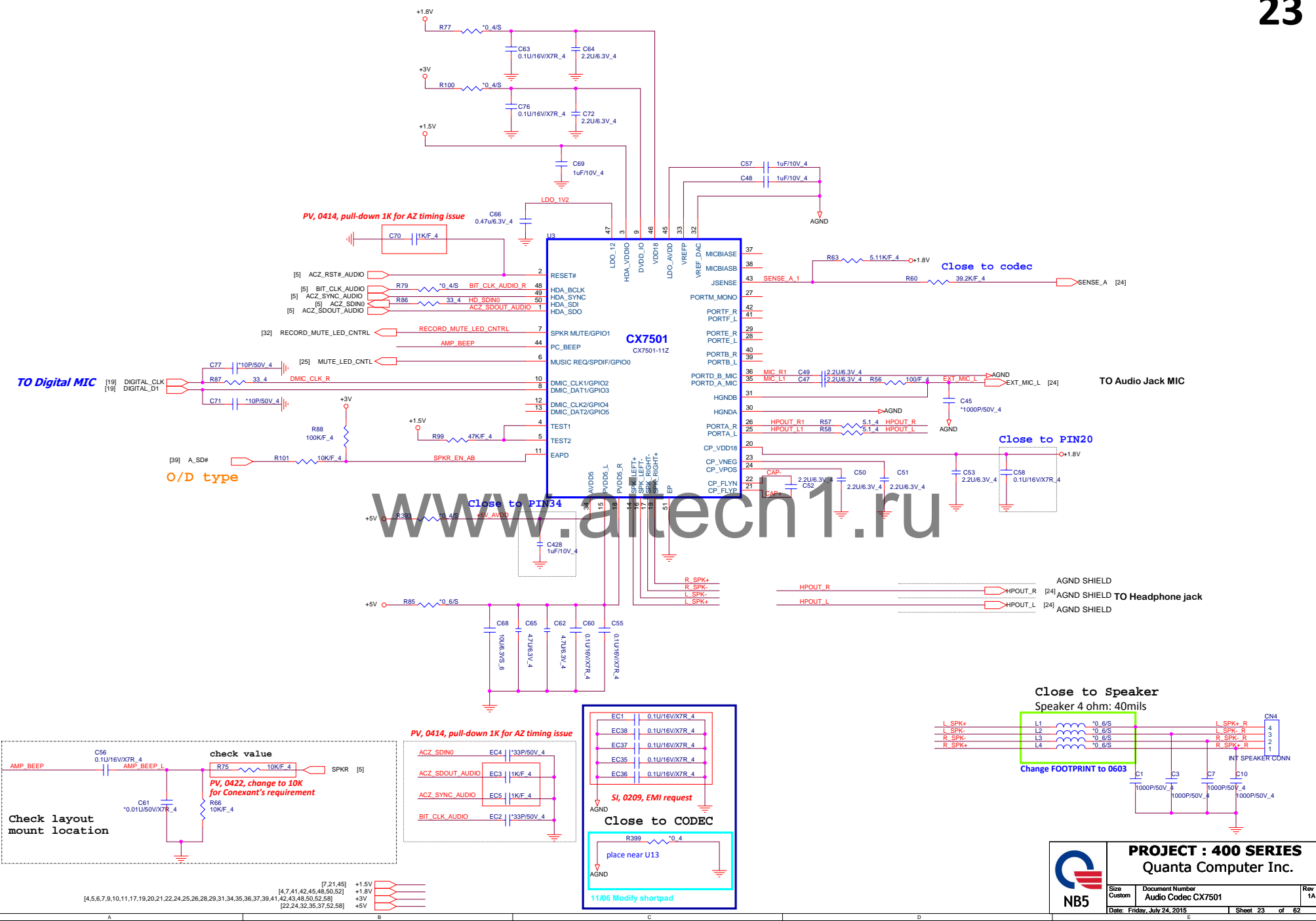


HDMI HPD SENSE



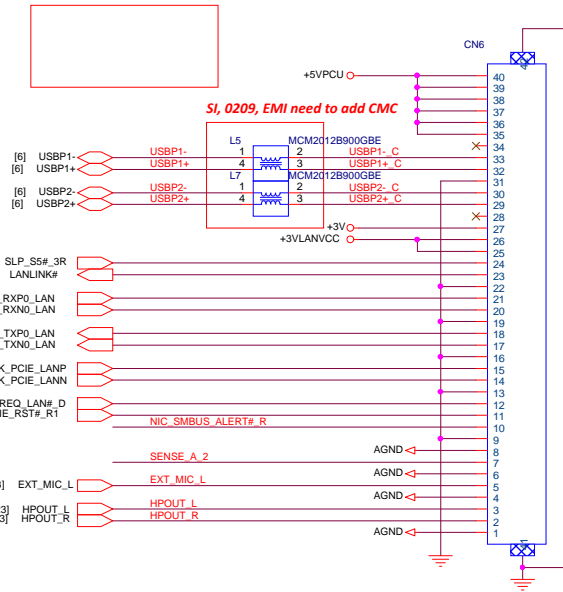
1028@RNY: follow X21 HPD circuit

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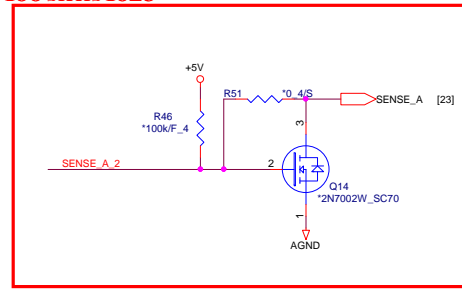
USB2.0 x2/LAN/Headphone_Mic Combo Jack Daughter Board Connector

PVR, 0720, delete USB 0 ohm co-lay

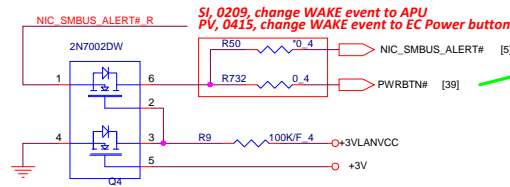


ALF@1025:
Following AMD Leading

400 series 1020



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SI, 0209, change WAKE event to APU
PV, 0415, change WAKE event to EC Power button

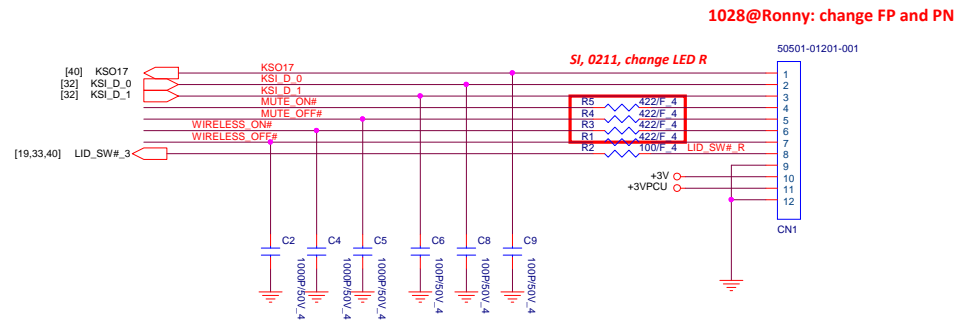
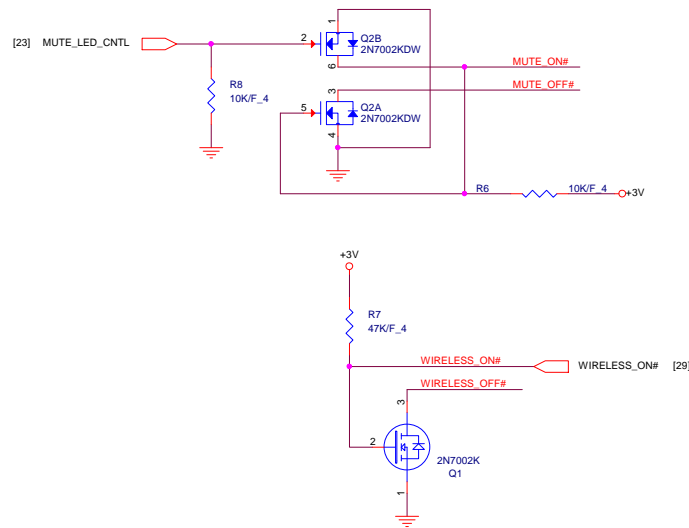
ALF@1031:
HP requested LAN PCIE wake to PWRBTN#

ALF@1031:
Needs to add 1 Pin for LAN Link to FCH.
Waiting for discussing with internal team



PROJECT : 400 SERIES
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Size	Document Number	Rev
Custom	Audio/USB BOARD	1A
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TPM (1.2 or 2.0)

26

ALF@1031:
Changed Power Nameing
1023@Ronny: follow Leading platform

1023@Ronny: follow Leading platform

ALF@1031:
Changed Power Nameing
SI, 0117, unstuff for double PU

ALF@1106:
When CZ, Stuff Q1


ALF@1106:
When CZ-L, Stuff R1

ALF@1118:
Following AMD Leading DB1.

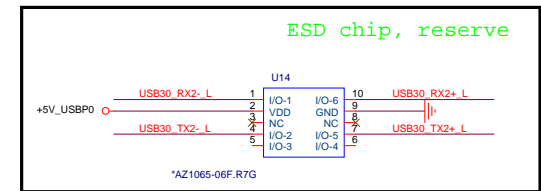
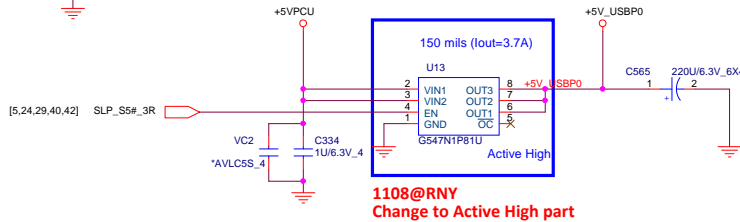
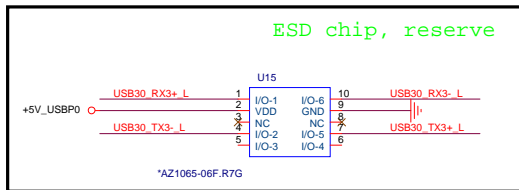
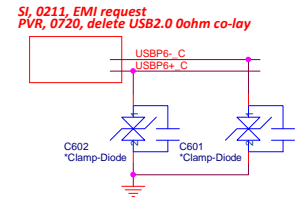
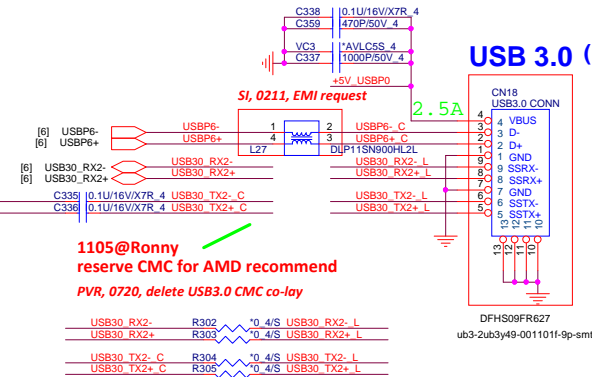
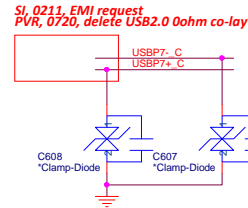
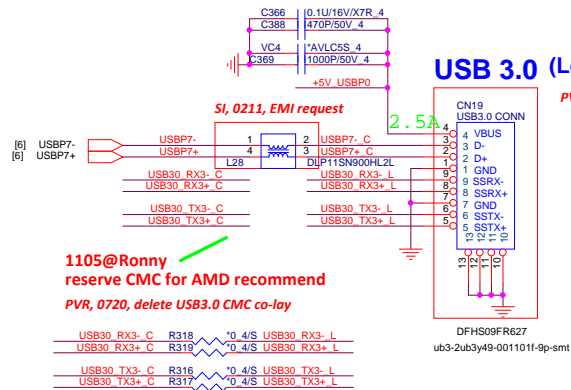
Need apply PN

ALF@1119:
Updated the QCI P/N
PV, 0415, update TPM PN with 06.40 FW

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			PROJECT : 400 SERIES Quanta Computer Inc.		
Size Custom	Document Number TPM SLB9665_QFN				Rev 1A
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USB 2.0/3.0 Combo



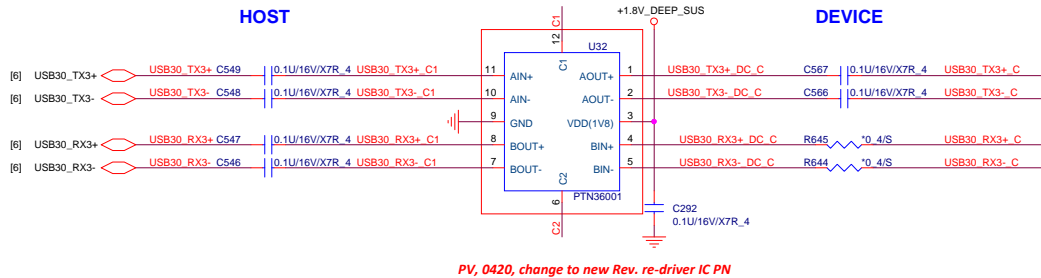
USB3.0

USB3.0 Re-driver IC

1016: Alfred
Added USB3.0 Re-driver for Lower Left.

USB3.0 re-driver IC

1121@RNY
Change USB3.0 re-driver to NXP solution



USB3.0 bypass 0 ohm

Layout Notes:
Stubs Trace less than 150mil

1112@ALF
Deleted the bypass way, due to the space limitation.

Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B		
			EQ[U]	DE[Z]	OS[Z]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel B		
			EQ[U]	DE[Z]	OS[Z]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

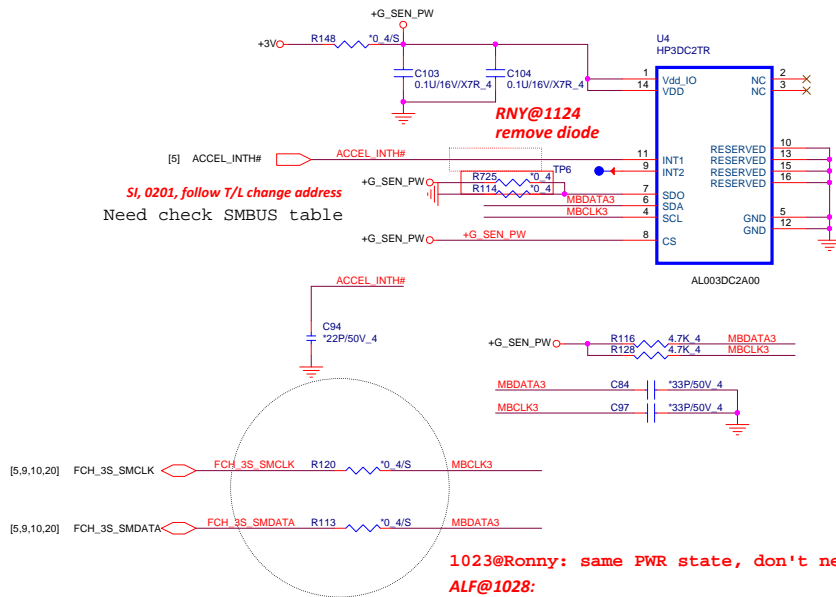
[24,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU
[7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU
[7,42,46,52,66] +1.8V_DEEP_SUS

PROJECT : 400 SERIES
Quanta Computer Inc.

Size Custom Document Number USB 3.0/USB3 Re-driver Rev 1A
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Accelerometer Sensor

G-Sensor Power need check



Touch screen

ALF@1028:
HP Confirmed, 400 Series AMD does NOT support the Touch Screen.

1023@Ronny: same PWR state, don't need MOS?

ALF@1028:
It is same Power Rail, can remove the LS MOSFET.


1028: *same Power Rail, can remove the LS MOSFET.*

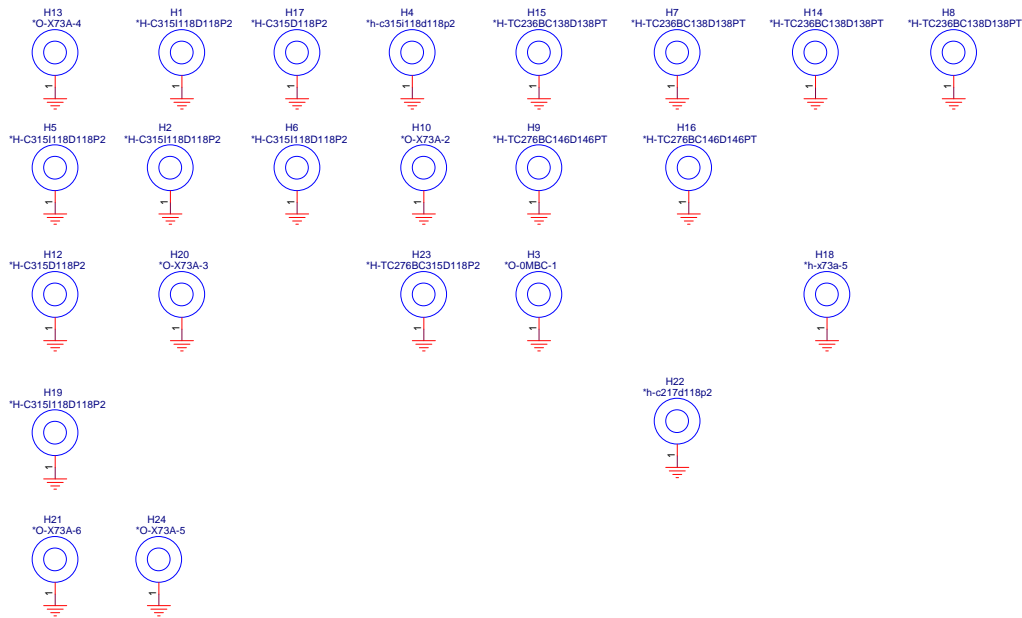
1028@Ronny:
need change pin define

ALF@1025:
400 Series AMD does Not support the WWAN.
So, Del the related WWAN_DET# components.

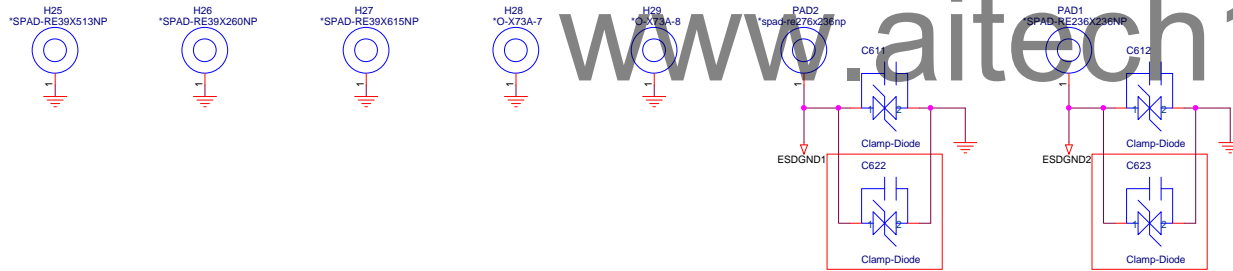
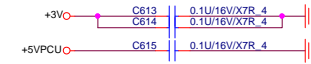
RNY@1209:
400 Series AMD does Not support the M.2 SSD

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 NB5		PROJECT : 400 SERIES Quanta Computer Inc.	
		Size Custom	Document Number WWAN NGFF or SSD
Date: Friday, July 24, 2015		Sheet 30 of 62	Rev 1A



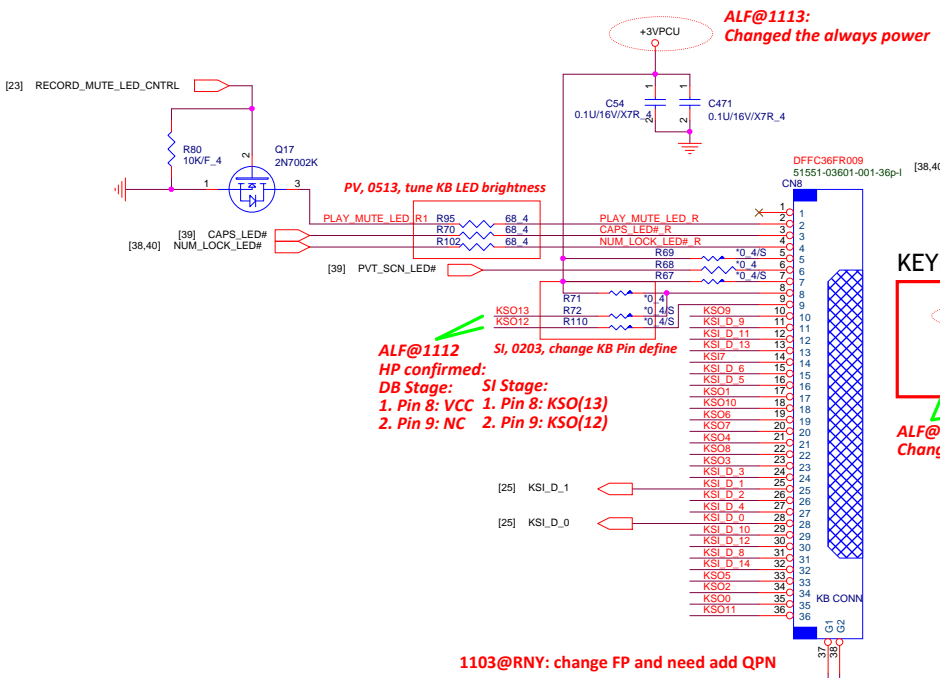
EMI CAP



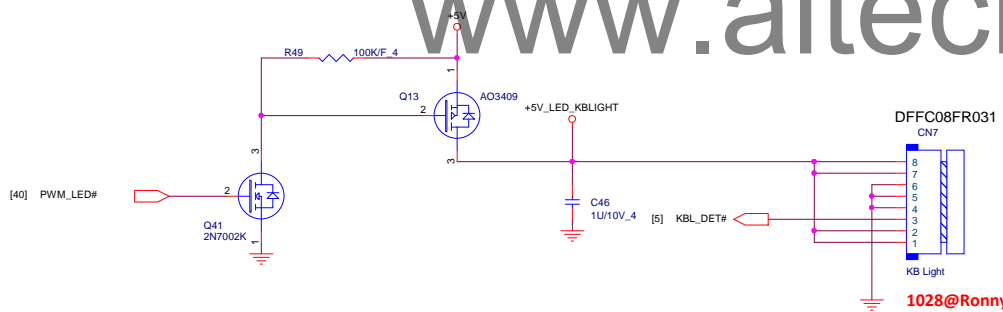
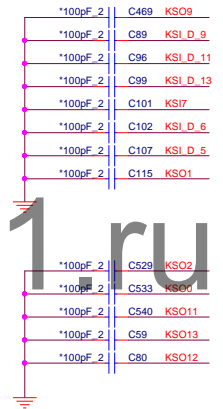
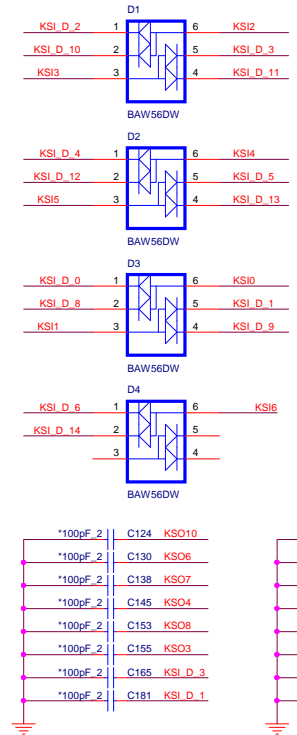
PV, 0422, reserve one more ESD part at each ESDGND
 PV, 0514, stuff varistor

	PROJECT : 400 SERIES Quanta Computer Inc.		
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KEYBOARD Con.



KEYBOARD PULL-UP



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Quanta Computer Inc.

Size Custom	Document Number KB/KB light	Rev 1A
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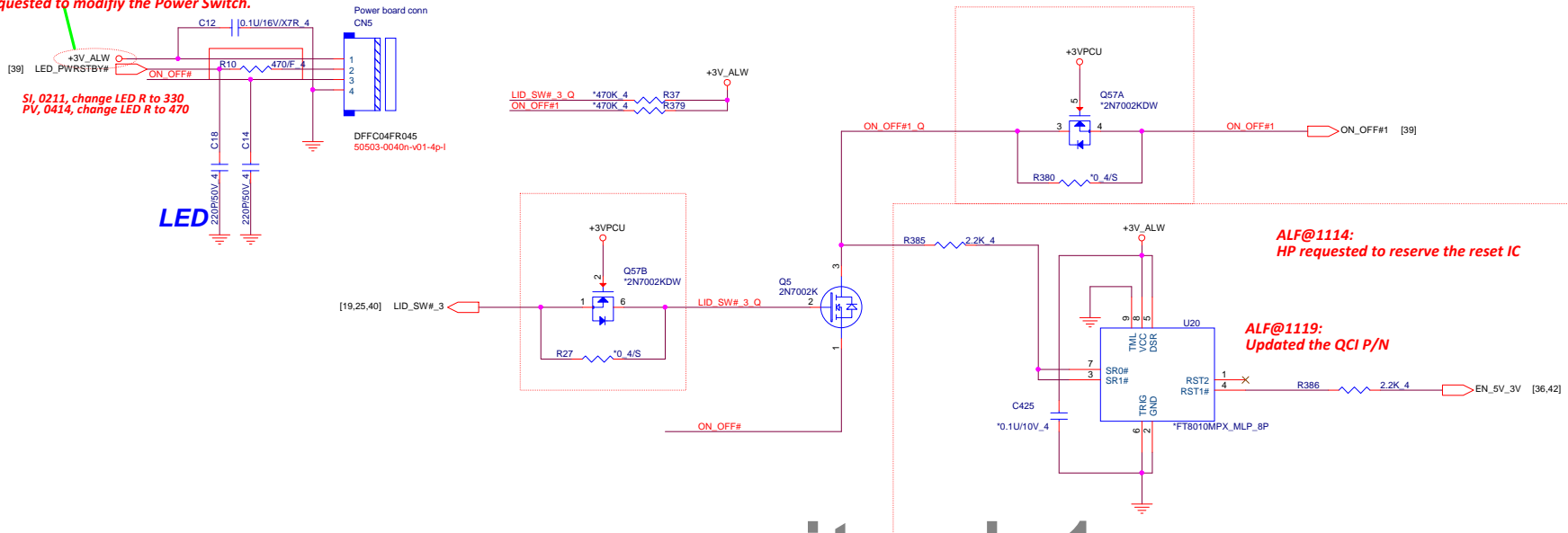
[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58] +3V
[22,23,24,35,37,52,58] +5V
[7,25,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

Power Button Connector

1112@RNY: change to 4Pin FP and PN

ALF@1115:

HP requested to modify the Power Switch.



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[42,43,44,57] +3V_ALW

[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58] +3V

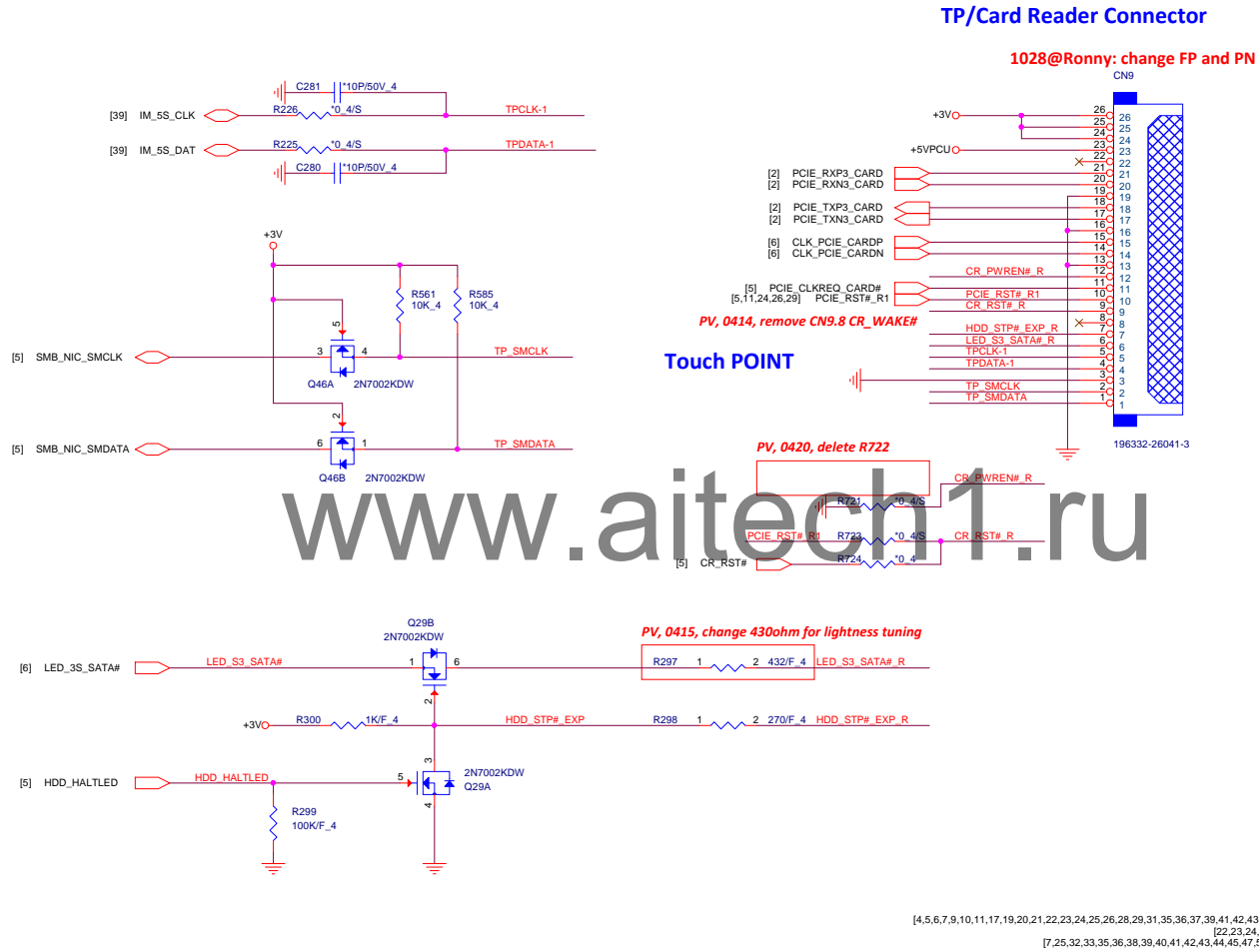
[22,23,24,32,35,37,52,58] +5V

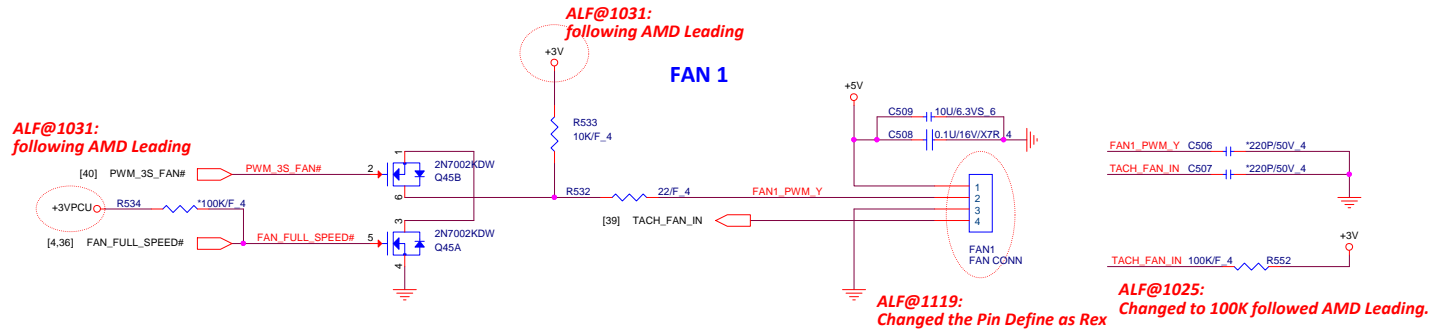
[7,25,32,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU



PROJECT : 400 SERIES
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Size	Document Number	Rev
Custom	33 -- PB/LID	1A
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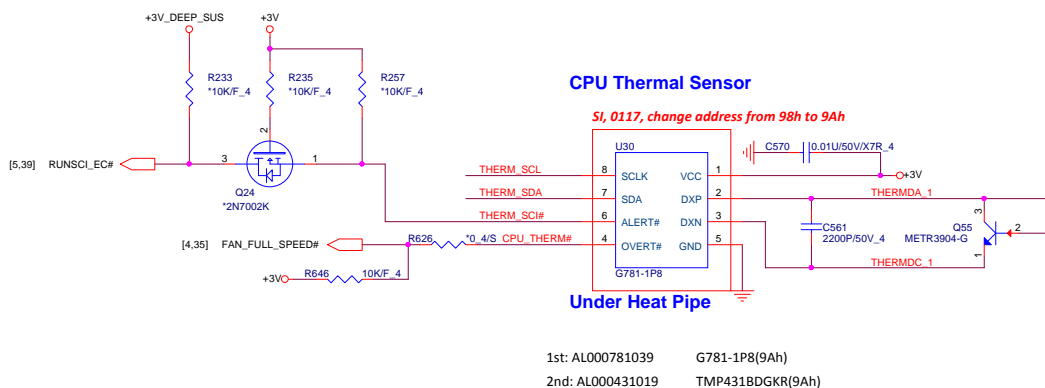
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[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,36,37,39,41,42,43,48,50,52,58] +3V
 [22,23,24,32,37,52,58] +5V
 [7,25,32,33,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU
 [24,27,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU

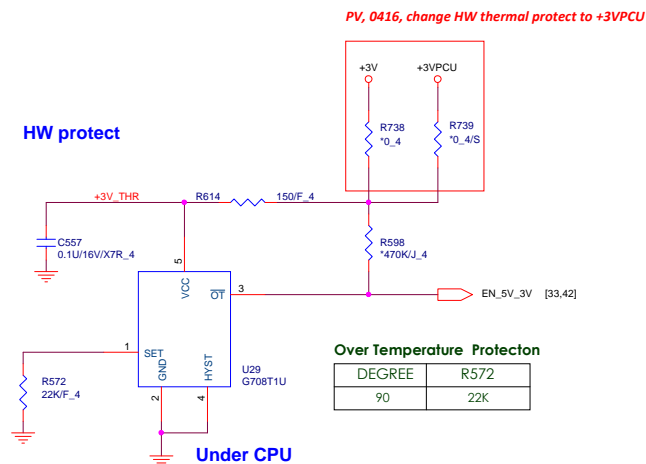


PROJECT : 400 SERIES
Quanta Computer Inc.

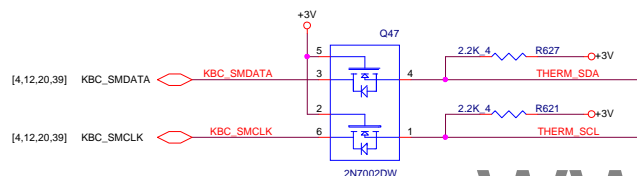
Size Custom	Document Number 35 -- FAN	Rev 1A
Date: Friday, July 24, 2015	Sheet 35 of 62	



HW protect



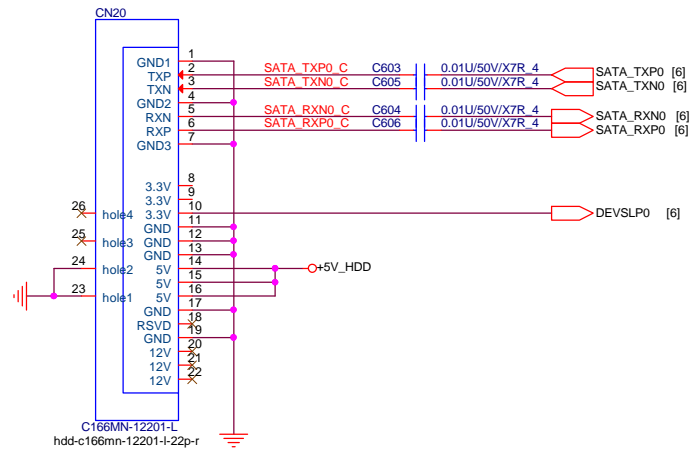
$$RSET \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$



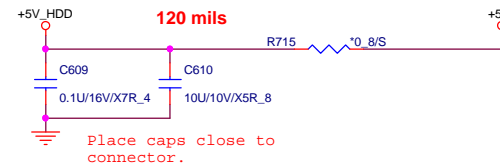
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[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,37,39,41,42,43,48,50,52,58] +3V
[7,25,32,33,35,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

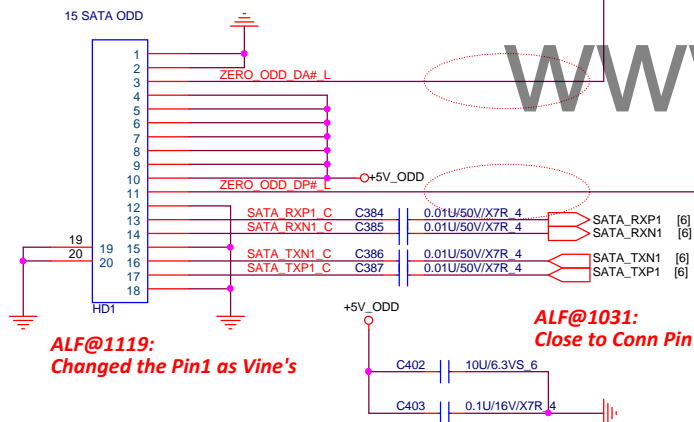
SATA-HDD



400 series 0929
Footprint and P/N TBD



SATA-ODD

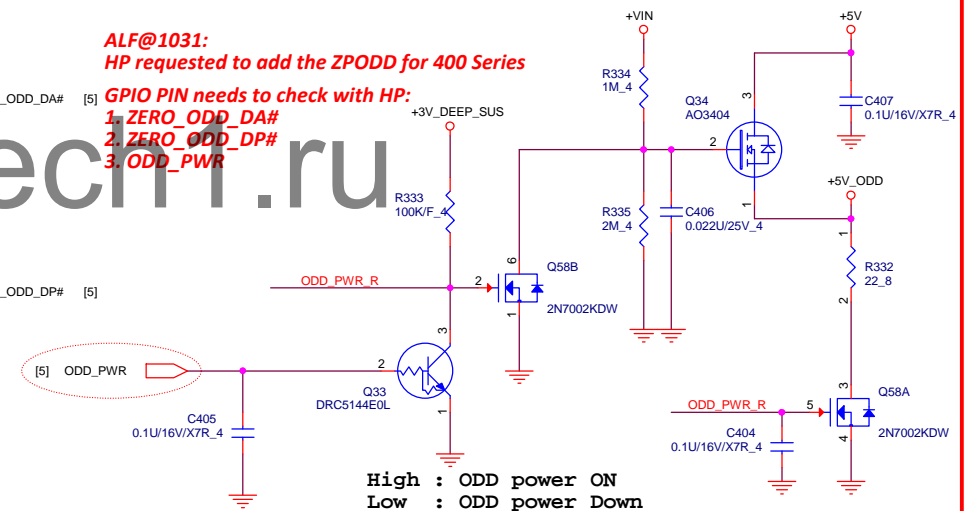


1028@Ronny: change to Vine 15" CONN

ALF@1031:
HP requested to add the ZPODD for 400 Series

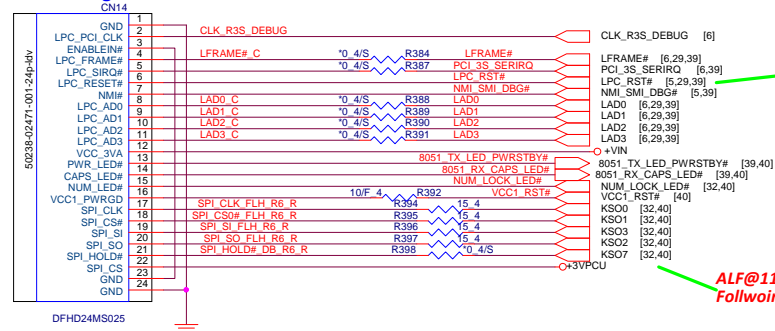
[5] ***GPIO PIN needs to check with HP:***

1. ZERO_ODD_DA#
2. ZERO_ODD_DP#
3. ODD_PWR



High : ODD power ON
Low : ODD power Down

EC debug conn.

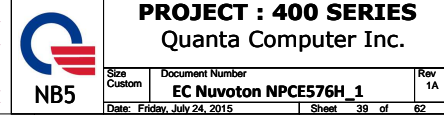


ALF@1027:
Following AMD Leading.

ALF@1115:
Following it in AMD Leading DB1.

1028@Ronny: change PN to DFHD24MS025

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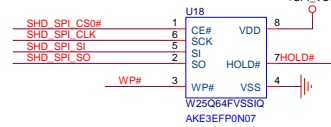




APU SPI ROM

Vender	Size	P/N (3.3V)	
WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
Socket		DG008000004	

U18&U19 footprint 要重疊

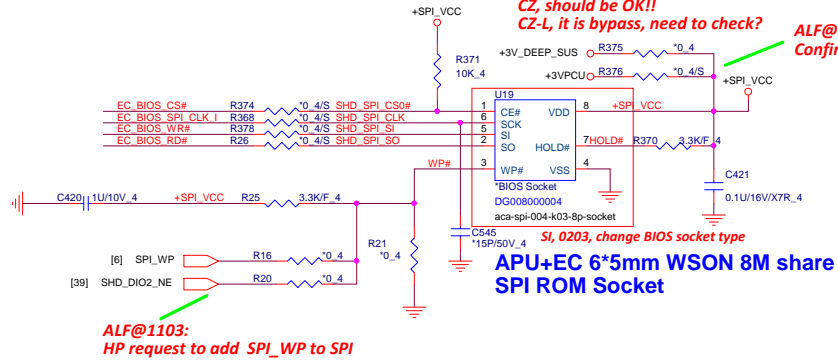


ALF@1031:
Needs to confirm EC Vendor, if use +3VPCU,
will it has leakage for APU from SPI Bus?
CZ, should be OK!!
CZ-L, it is bypass, need to check?

ALF@1113:
Confirmed HP, SPI Power Rail same as EC.

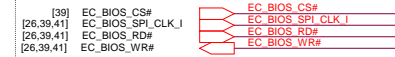
Alfred@1015:
Add flash ROM for first bring up (2MB ROM)
EC 6*5mm WSON 8M
SPI ROM Socket

SI, 0203, remove EC debug ROM



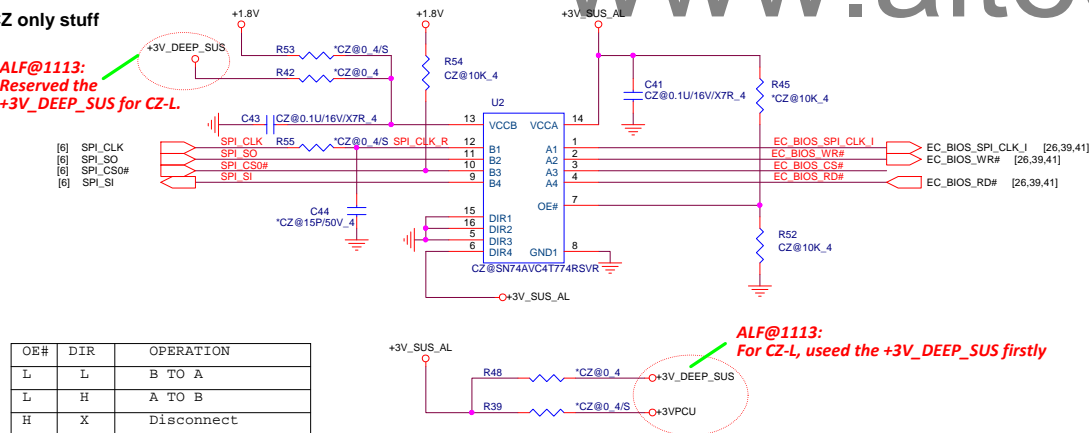
**APU+EC 6*5mm WSON 8M share
SPI ROM Socket**

From EC



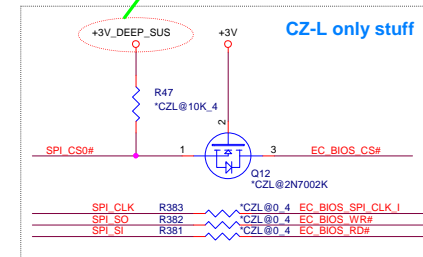
CZ only stuff

ALF@1113:
Reserved the
+3V_DEEP_SUS for CZ-L.



OE#	DIR	OPERATION
L	L	B TO A
L	H	A TO B
H	X	Disconnect

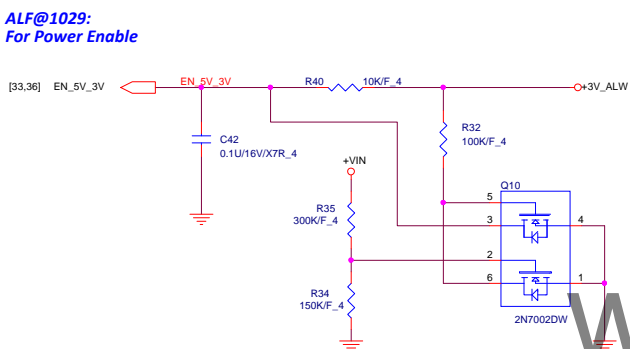
ALF@1113:
1. SPI bus isolation to FCH



		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number Flash(KBC+PCH)	Rev 1A	
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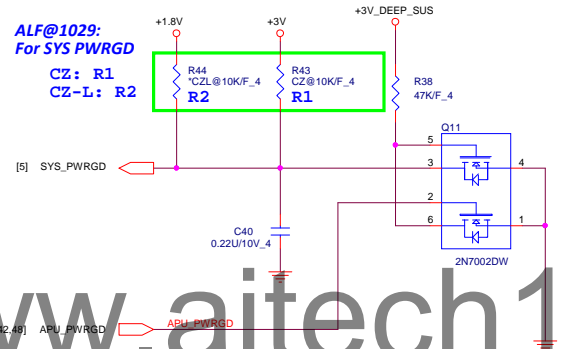
ALF@1114:
Deleted the circuit of PWROK Generate followed T/L Leading.

ALF@1029:
For Power Enable

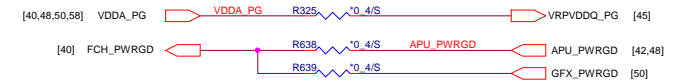


ALF@1029:
For SYS PWROGD

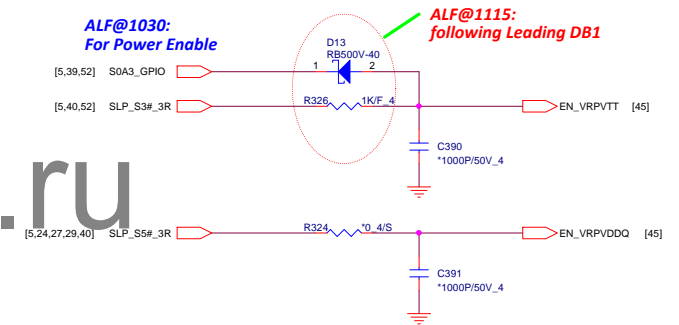
CZ: R1
CZ-L: R2



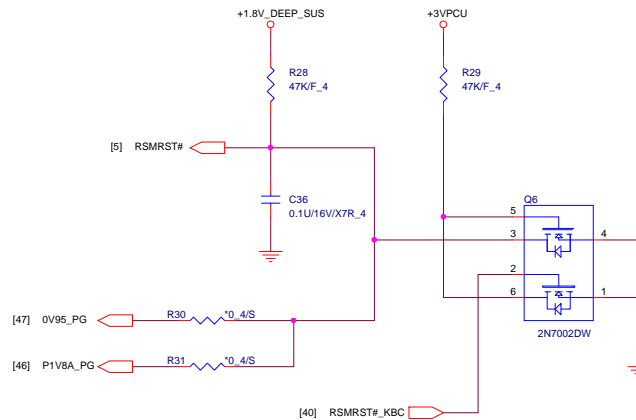
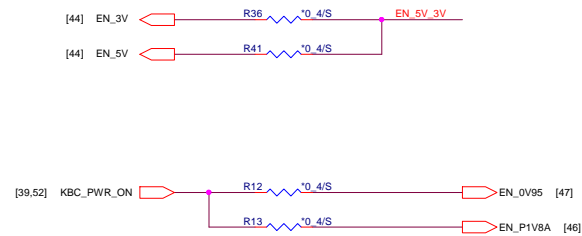
ALF@1030:
For System PG



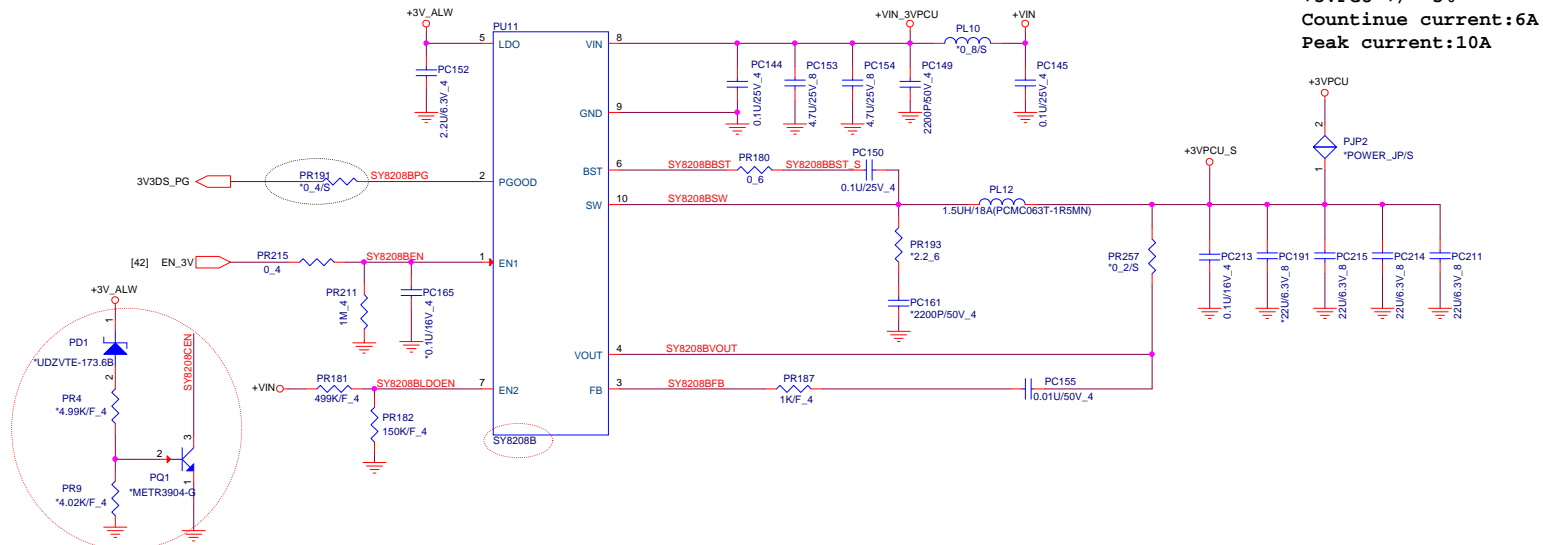
ALF@1030:
For Power Enable



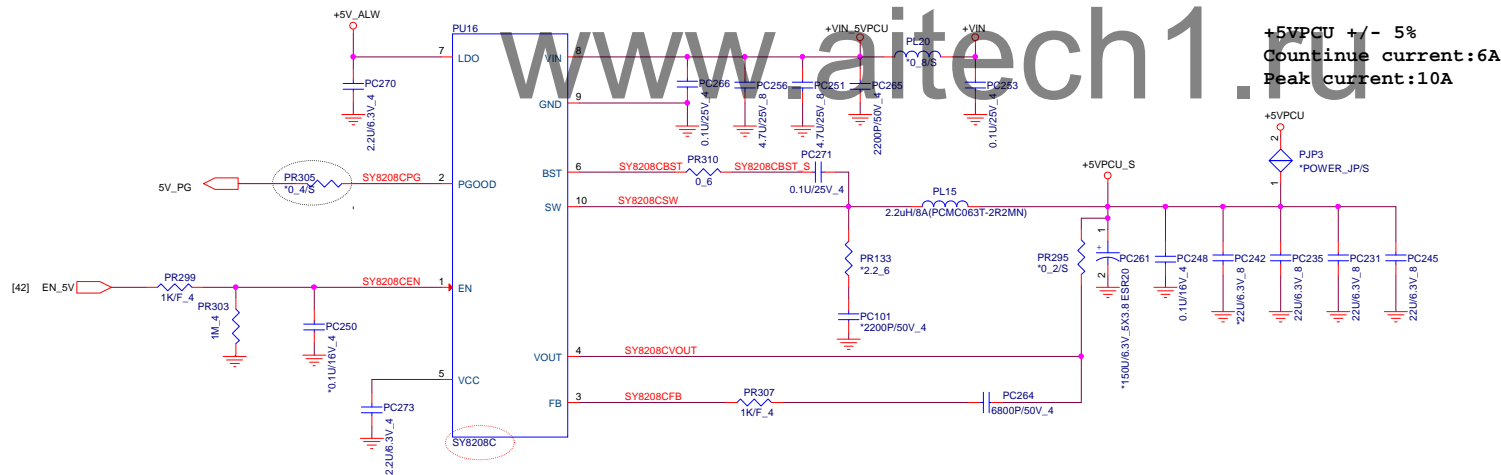
ALF@1115:
following Leading DB1



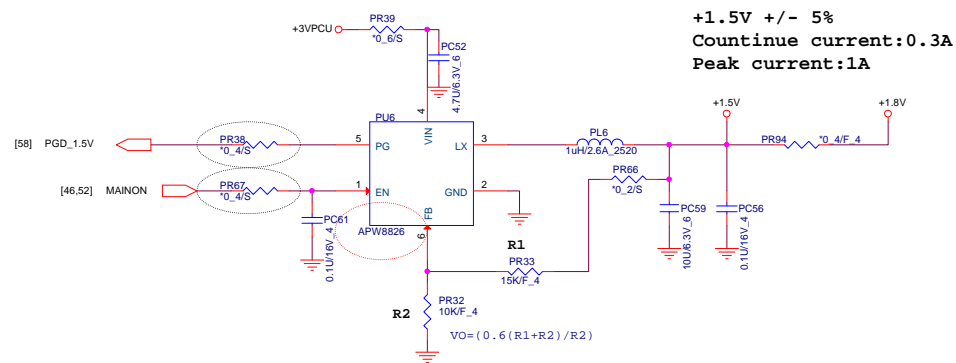
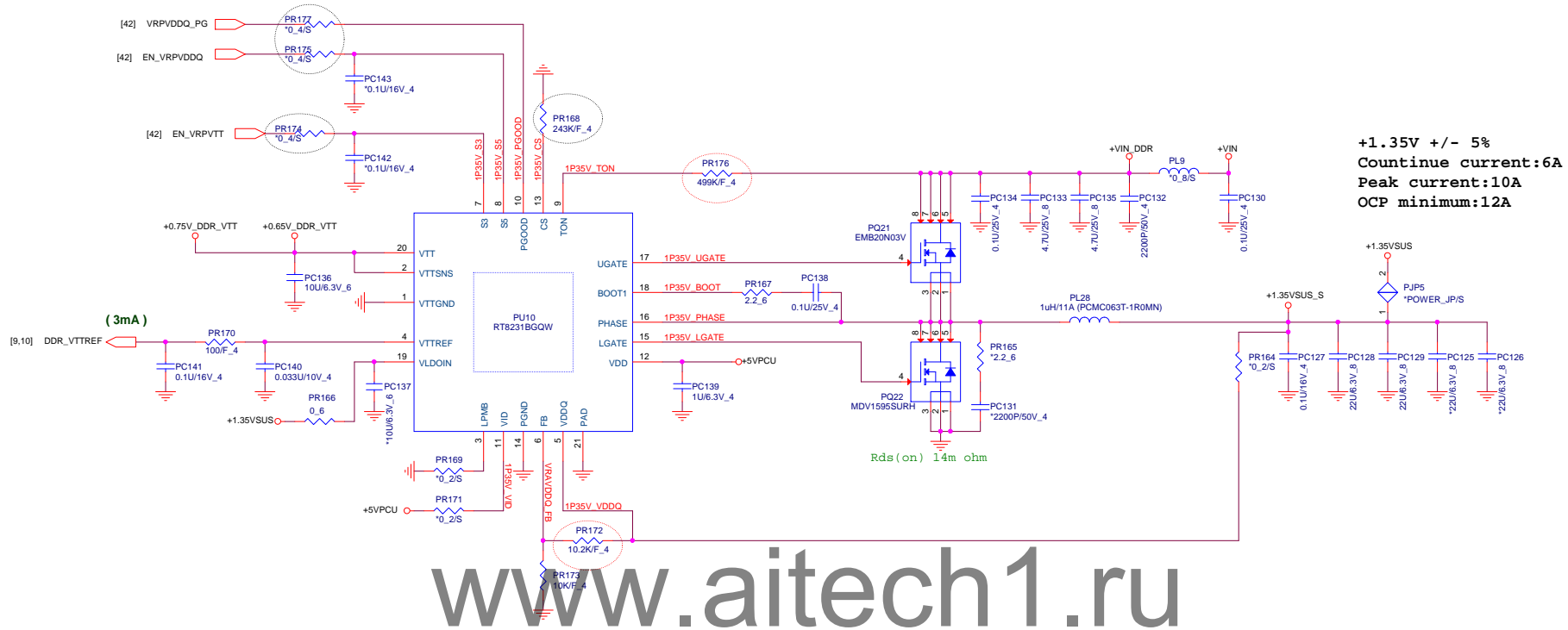
Do Not add test pad
on +3VPCU



+3VPCU [7,25,32,33,35,36,38,39,40,41,42,43,45,47,52,55,57]
 +5VPCU [24,27,31,34,43,45,46,47,48,50,52,53,55,56,58]

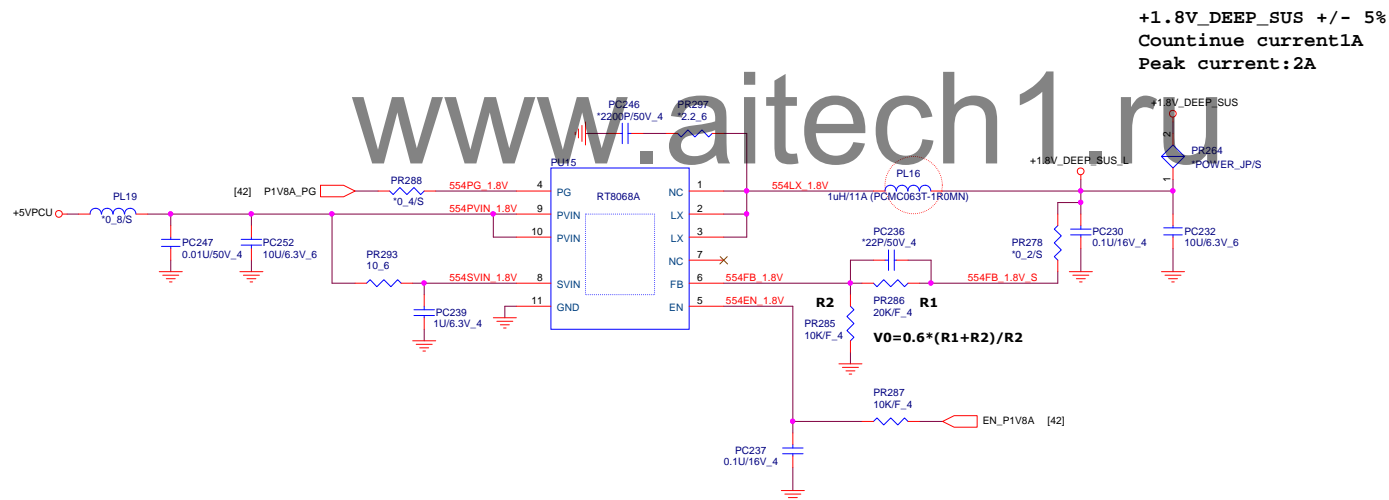
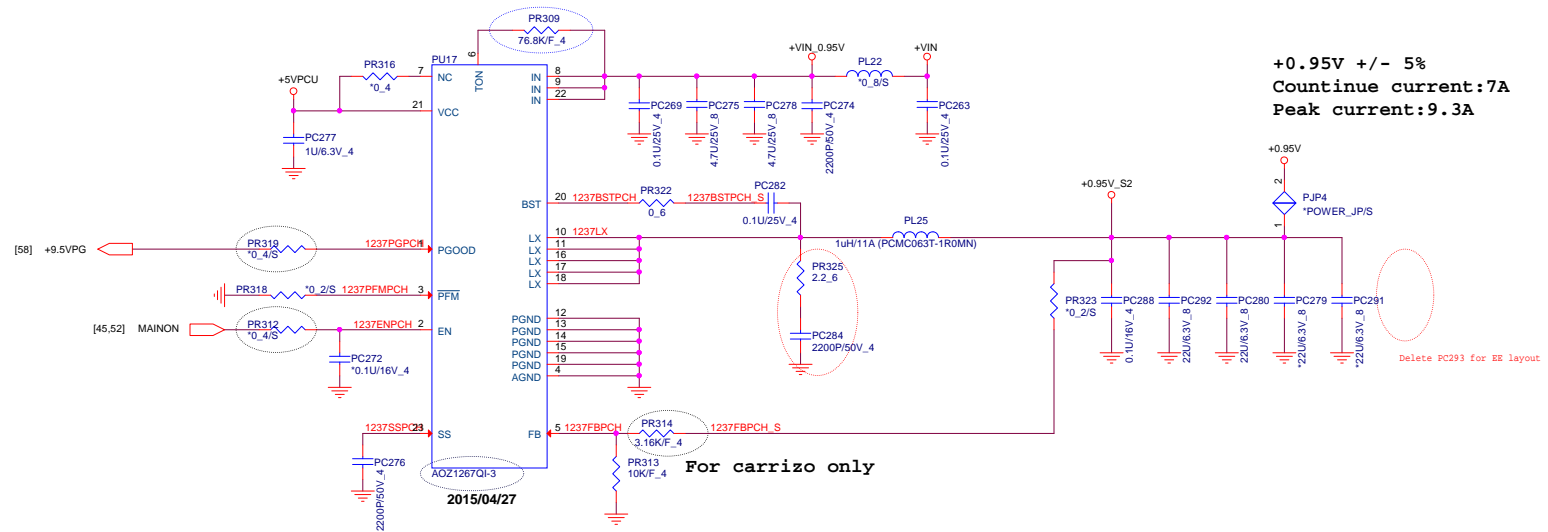


PROJECT : 400 SERIES			
Quanta Computer Inc.			
Size	Document Number	Rev	
Custom	3/5VPCU(RT8243A)	1A	
Date	Friday, July 24, 2015	Sheet	44 of 62



+1.35VSUS [3,7,9,10]

PROJECT : 400 SERIES			
Quanta Computer Inc.			
NB5	Size	Document Number	Rev
	DR3	RT8231B/1.8VS5	1A
Friday, July 10, 2015		45Sheet	of 62



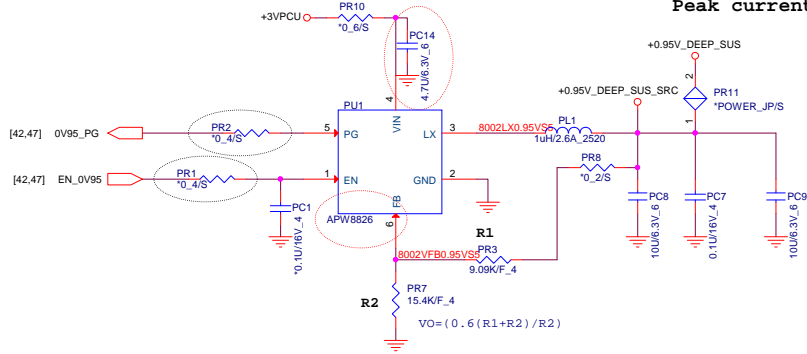
+VIN [19,37,38,42,43,44,45,47,49,51,54,56]
 +3VPCU [7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,53]
 +5VPCU [24,27,31,34,43,44,45,47,48,50,52,53,55,56,58]



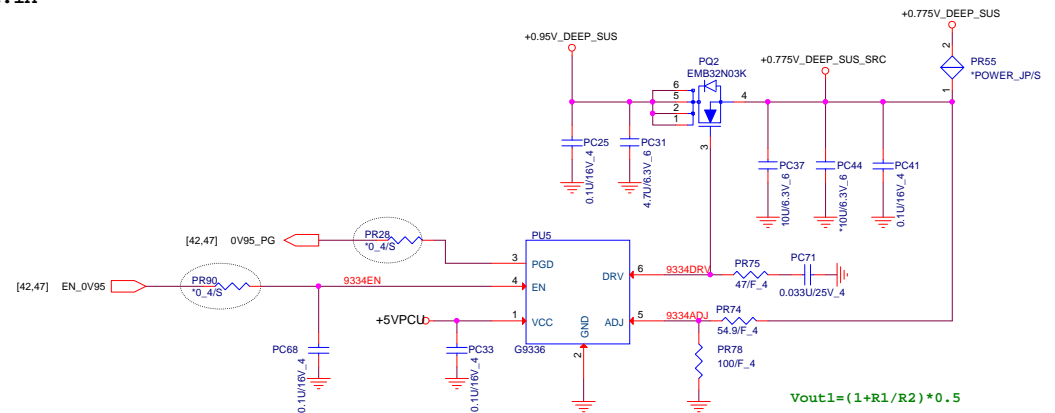
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Friday, July 24, 2015	Sheet#6 of 62	

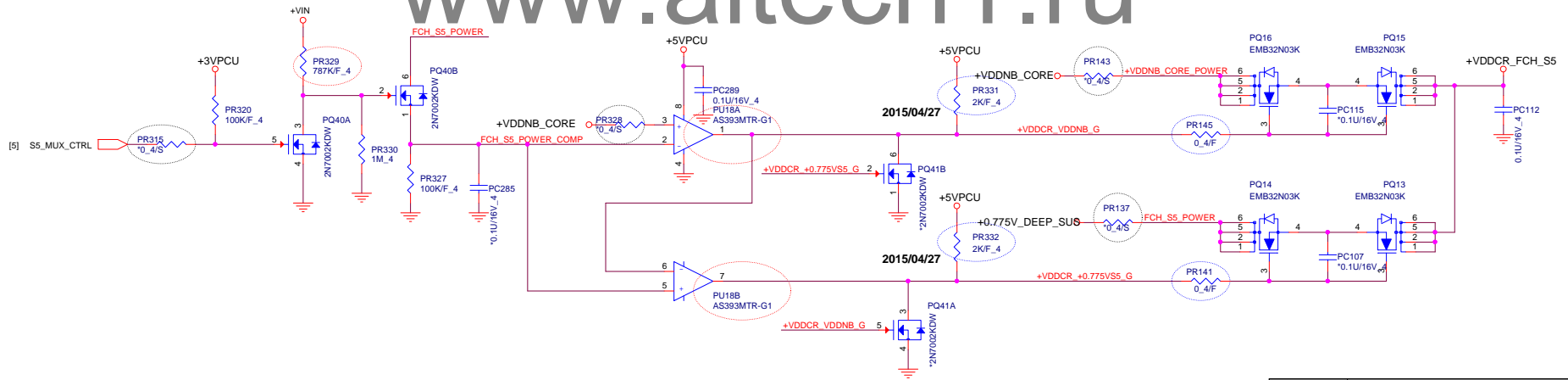
+0.95V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A



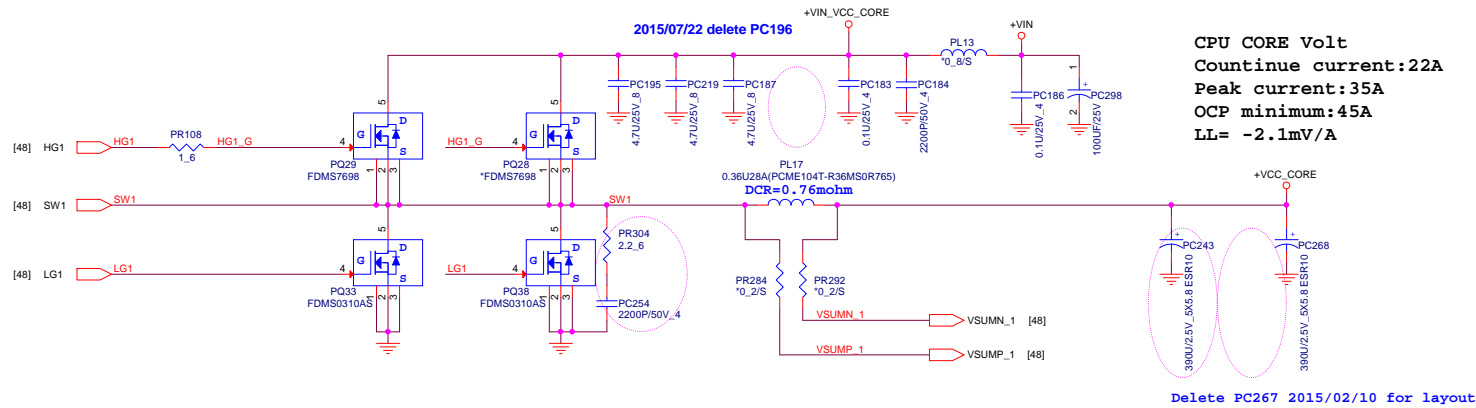
+0.775V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A



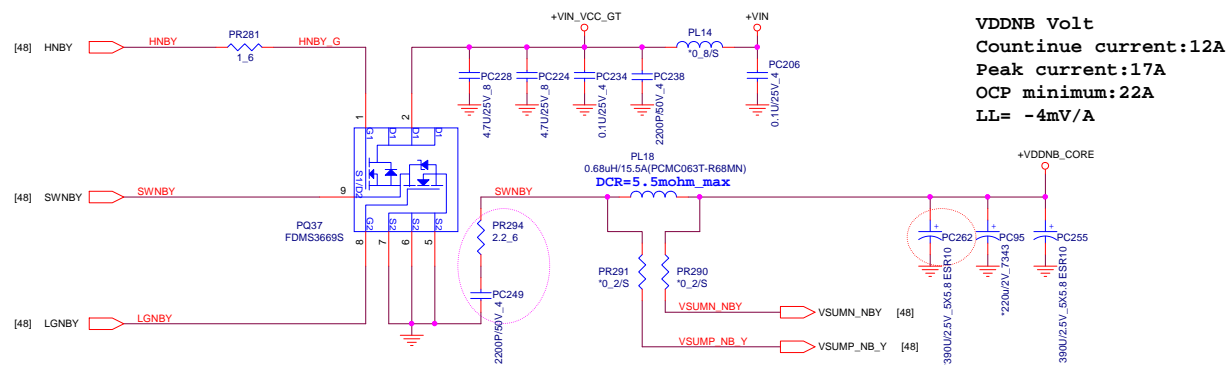
www.aitech1.ru





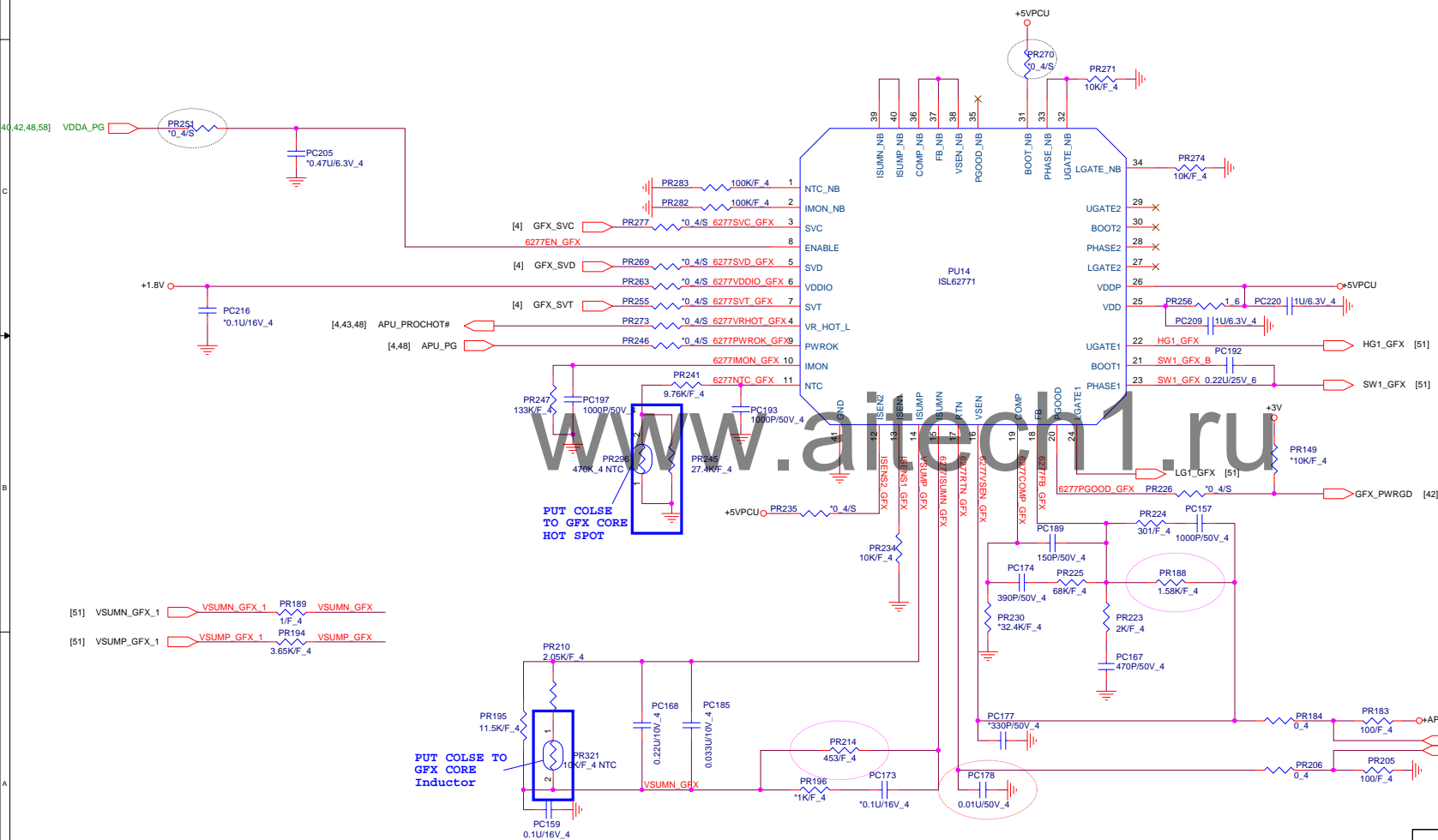


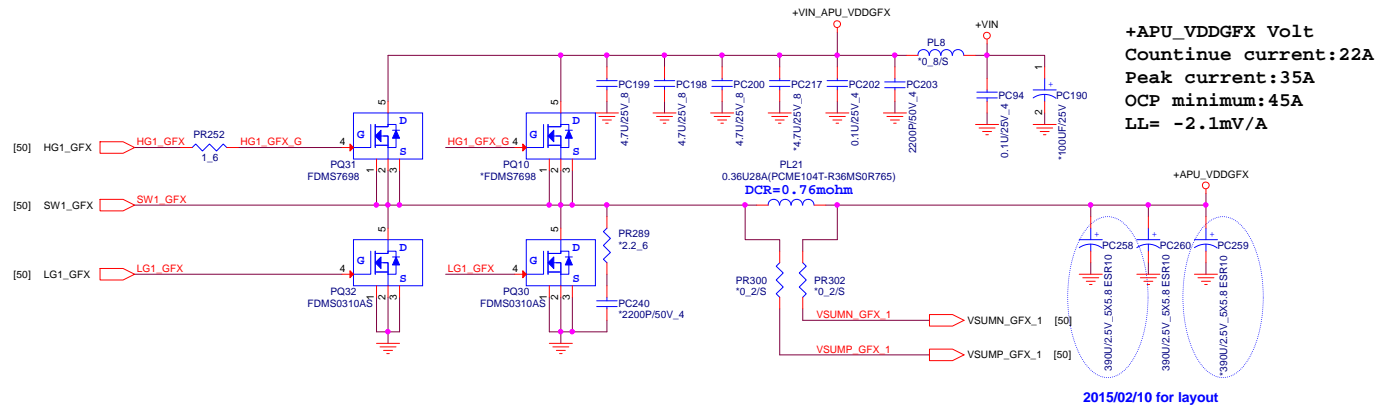
www.aitech1.ru



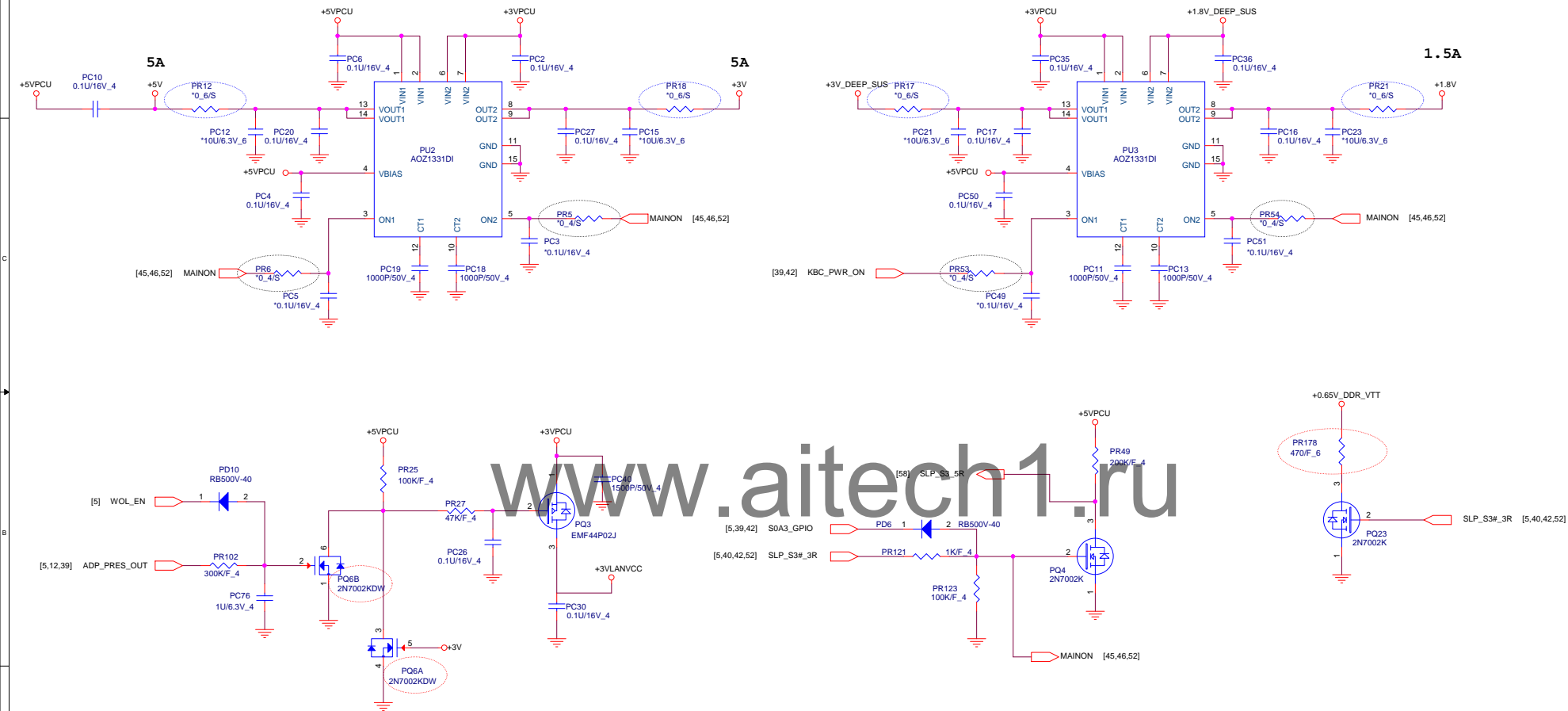
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core2	1A
Date: Friday, July 24, 2015	Sheet 9 of 62	






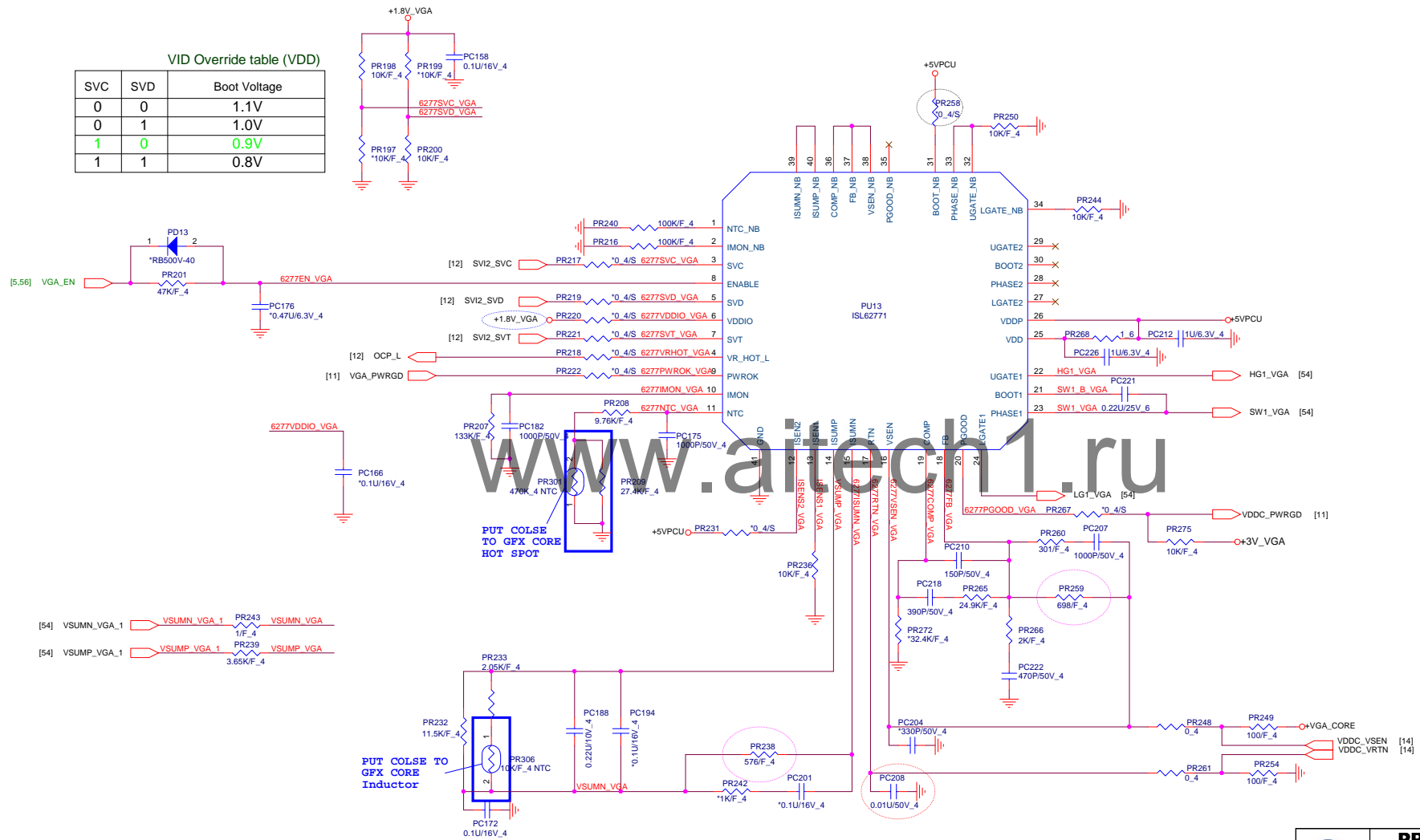
www.aitech1.ru

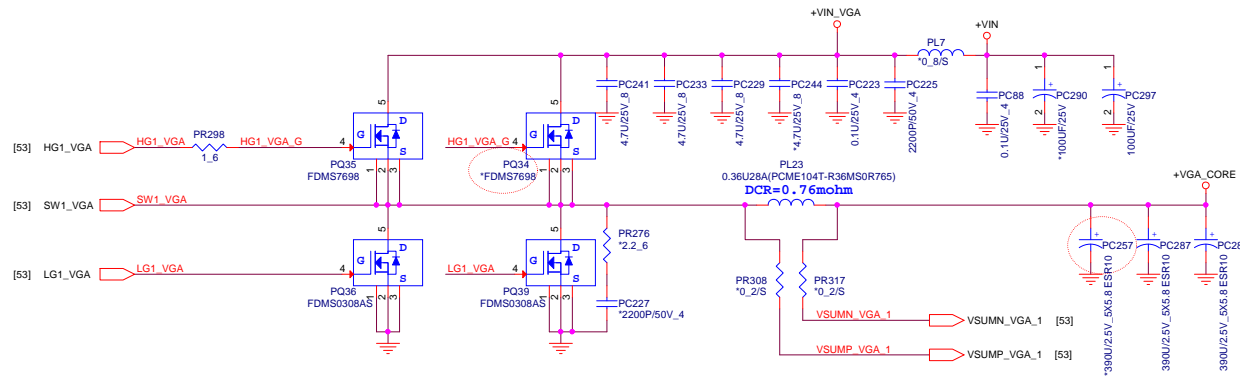


[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,58] +3V
 [22,23,24,32,35,37,58] +5V
 [19,37,38,42,43,44,45,46,47,49,51,54,56] +VIN
 [7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,55,57] +3VPCU
 [24,27,31,34,43,44,45,46,47,48,50,53,55,56,58] +5VPCU
 [24] +3VLAVCC

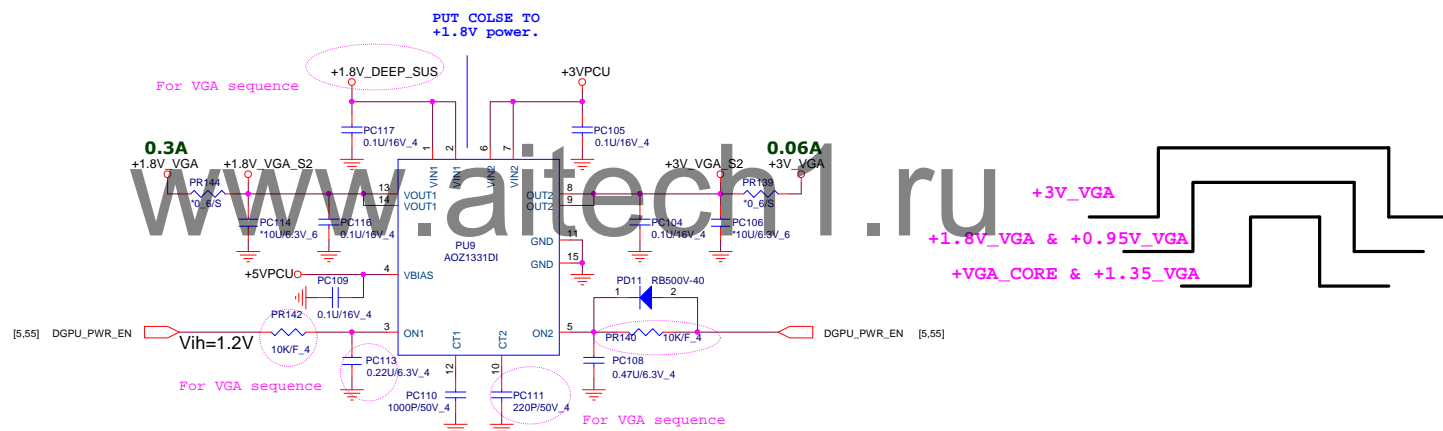
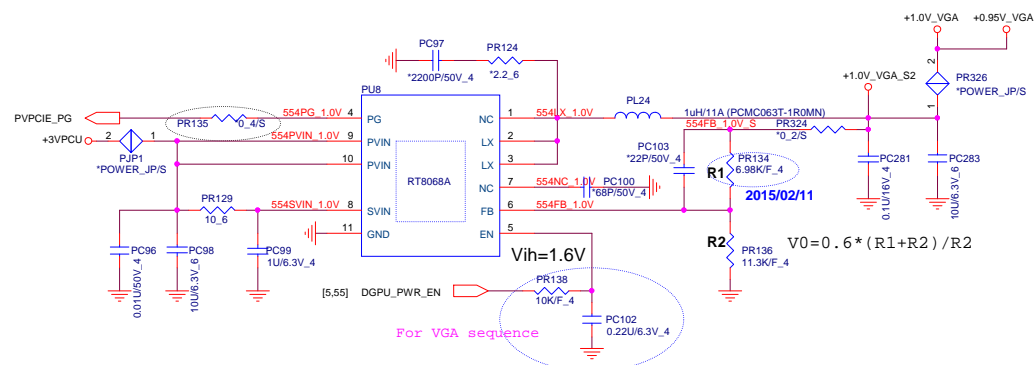
		PROJECT : 400 SERIES	
		Dis-charge IC (SLG55448)	
Size Custom	Document Number	Rev 1A	
Date: Friday, July 24, 2015	Sheet 62	of	62

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

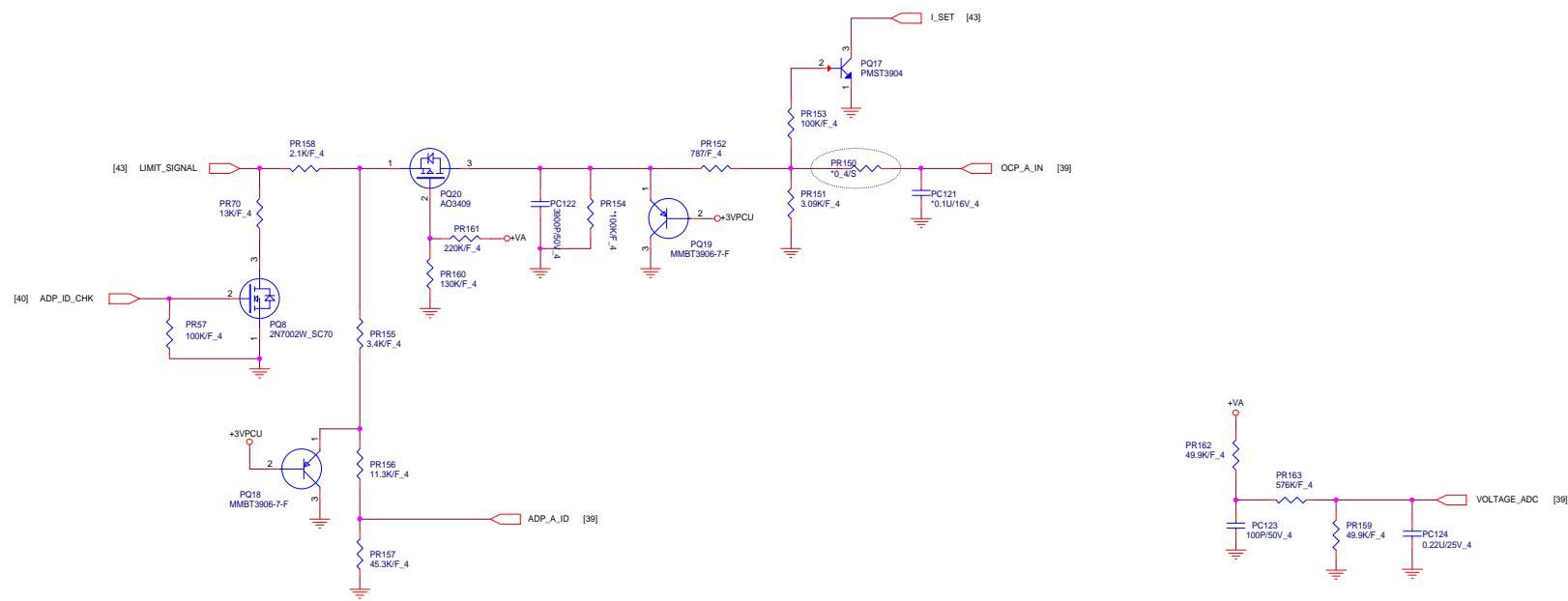




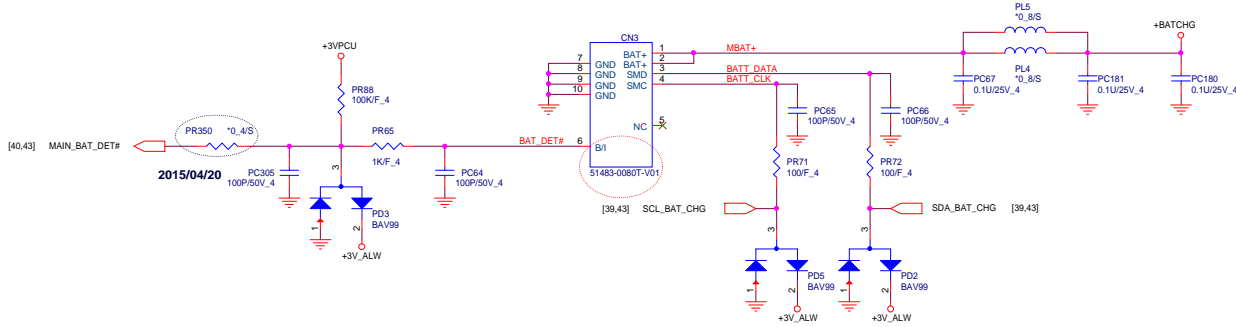
www.aitech1.ru

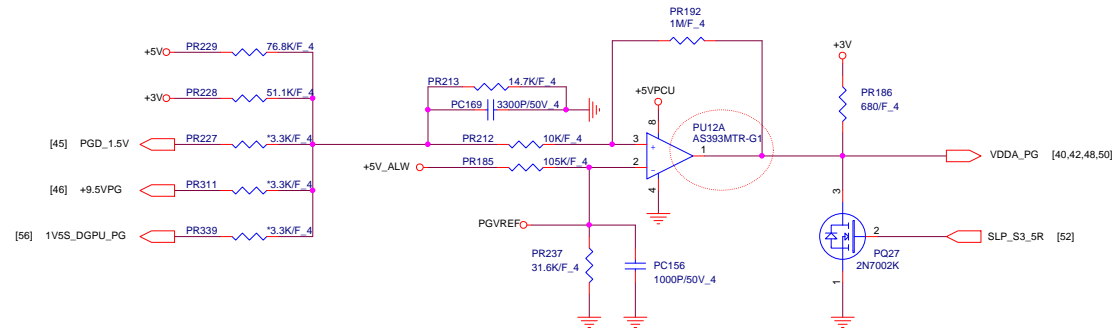






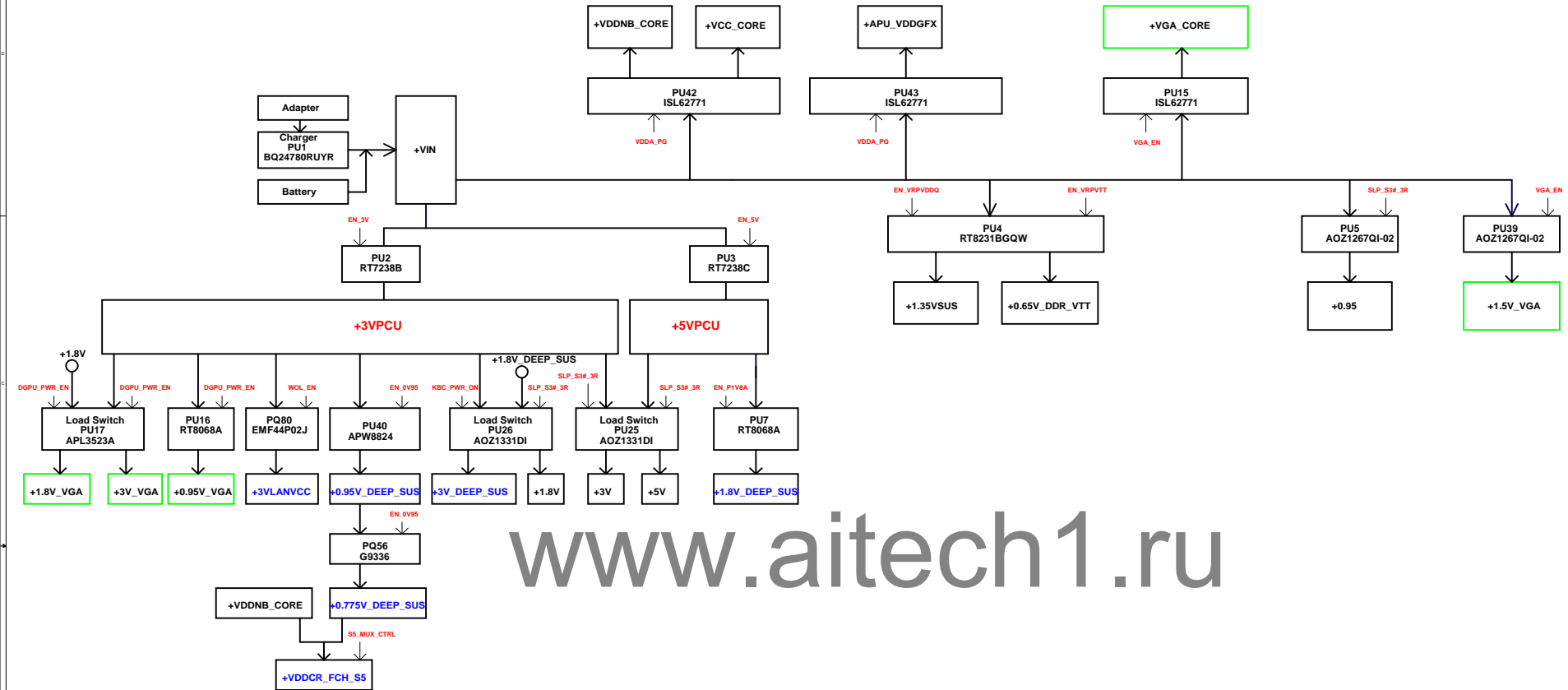
www.aitech1.ru





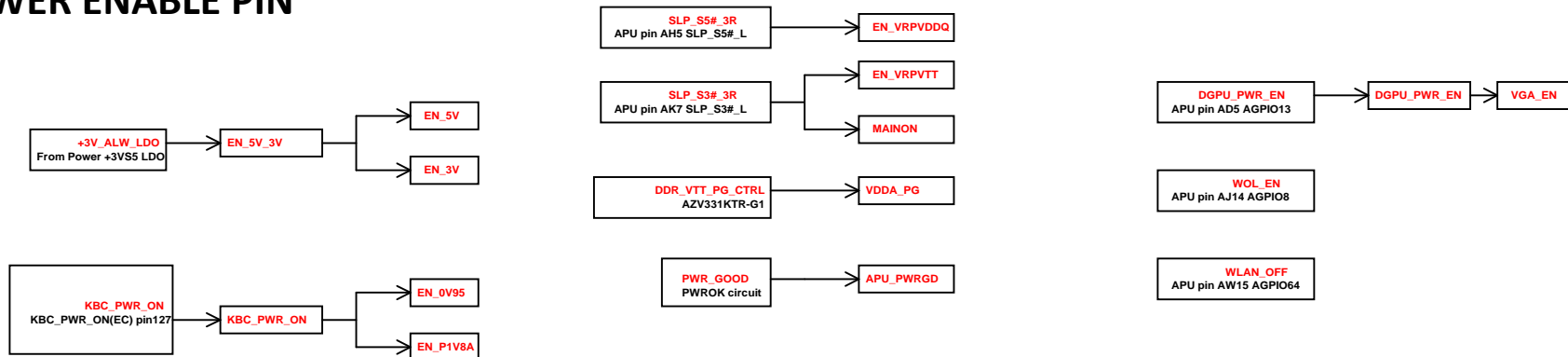
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POWER BLOCK DIAGRAM



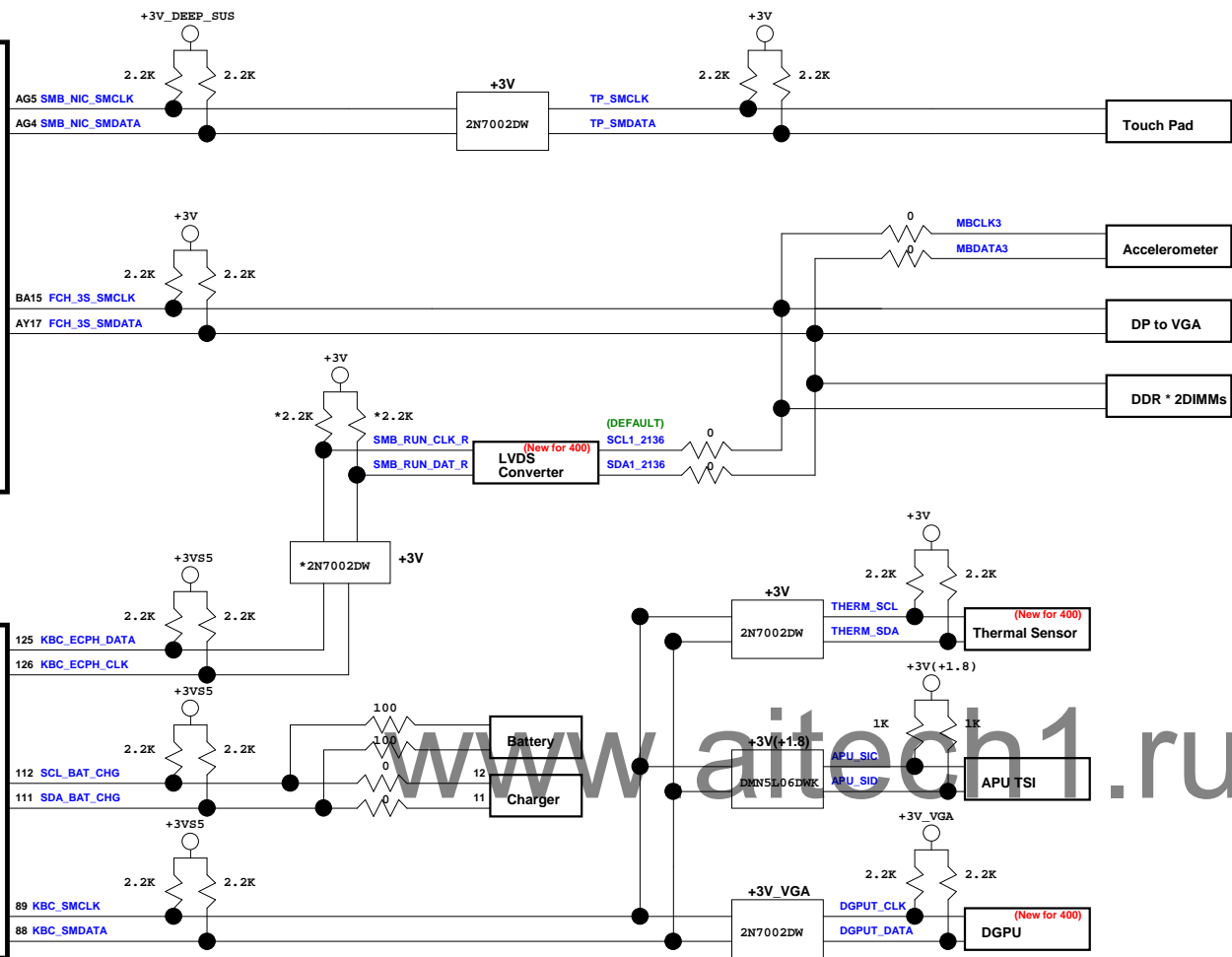
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POWER ENABLE PIN



Carrizo (L)

EC
NPCE586H



HSIO Lane	Port Assignment
USB3 #0	NC
USB3 #1	NC
USB3 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3	USB2.0/USB3.0 Combo Jack(Left side down)
PCIE0	NIC
PCIE1	WLAN
PCIE2	NC
PCIE4	Cardreader (PCIE)
DDI0	eDP
DDI1	DP2VGA(CZ) / DP2HDMI(CZ-L)
DDI2	HDMI(CZ)
SATA0	HDD / BOM 0 ohm Option for M.2 SSD
SATA1	ODD
PEG0~3	dGPU
PEG4~7	NC

USB2.0	Port Assignment
USB2 #0	Camera
USB2 #1	USB2.0(Right side on USB Board)
USB2 #2	USB2.0(Right side on USB Board)
USB2 #3	NC
USB2 #4	Bluetooth
USB2 #5	Finger Print
USB2 #6	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #7	USB2.0/USB3.0 Combo Jack(Left side down)

[illegible][illegible]

UMA/DIS SKU TABLE

When setup the BOM, please make sure every item are finalized or not !

Schematic Value Note:

* is NO SMT part (empty)

DIS@ : for VGA mode

CZ@ : for Carrizo

CZL@ : for Carrizo-L

Function	Carrizo UMA	Carrizo-L UMA	Discrete	Page
GPU				
APU side PEG cap	NoASM	NoASM	ASM	02
GPU circuit	NoASM	NoASM	ASM	11,12,13,14,
GPU Power circuit	NoASM	NoASM	ASM	15,16
				53,54,55,56
GPU enable circuit				
C143	NoASM	NoASM	ASM	05
C470	NoASM	NoASM	ASM	
D16	NoASM	NoASM	ASM	
D17	NoASM	NoASM	ASM	
Q21	NoASM	NoASM	ASM	
R160	NoASM	NoASM	ASM	
R454	NoASM	NoASM	ASM	
VBIO ID				
R76	ASM	ASM	NoASM	05
R98	ASM	ASM	NoASM	
R82	NoASM	NoASM	ASM	
R105	NoASM	NoASM	ASM	
APU VDDP GFX rail				
C122	ASM	NoASM	ASM	07
C436	ASM	NoASM	ASM	
R402	ASM	NoASM	ASM	
R155	NoASM	ASM	NoASM	

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